

DesignCon 2005

Connector footprint optimization enables 10 Gb+ signal transmission

Jan De Geest, PhD
Winnie Heyvaert
Stefaan Sercu, PhD
Dana Bergey

FCI
Communications, Data, Consumer Division
FCI 's-Hertogenbosch BV
Victorialaan 1
5213 JG 's-Hertogenbosch
The Netherlands
Tel.: +31 73 6206 922
E-mail: jdegeest@fciconnect.com
wheyvaert@fciconnect.com
ssercu@fciconnect.com
dbergey@fciconnect.com

Abstract

Hardware designers have multiple options available to improve system performance by optimizing each component within their design. In recent years, each of the components of an interconnection link has been addressed, as the focus continually shifts towards the next obstacle to higher-speed transmission. Today, a primary barrier to increasing data rates is the transition between connectors and PCBs, or the connector footprint. This paper illustrates how surface mount (SMT) connectors enable further optimization of system performance, thereby breaking through this latest speed barrier. Real-world applications are analyzed, showing the benefits and issues of SMT connectors.

Author's biographies

Jan De Geest was born in Gent, Belgium on July 30, 1971. He received the degree in electrical engineering from the University of Gent, Belgium in 1994 and the degree in supplementary studies in aerospace techniques from the University of Brussels, Belgium in 1995. He was the recipient of the 1995 Best Thesis Award presented by the Flemish Aerospace Group (FLAG). From September 1995 to December 1999 he worked as a research assistant at the Department of Information Technology (INTEC) of the University of Gent, where he received the PhD degree in electrical engineering in 2000. Since January 2000 he has been working for FCI CDC in 's-Hertogenbosch, The Netherlands. His work focuses on the modeling and simulation of high-speed interconnection links. He has authored and co-authored over 25 technical papers in international journals and international conference proceedings.

Winnie Heyvaert was born in Aalst, Belgium on December 18, 1971. She received the degree in electrical engineering from the University of Gent, Belgium in 1996. From 1996 to 1998, she worked as a research assistant at the Department of Information Technology (INTEC) of the University of Gent, studying the effects of mobile phone radiation. In September 1998, she joined FCI CDC in 's-Hertogenbosch, the Netherlands. From 1998 up to 2002, she worked on fiber-optic communication. In October 2002, she joined the signal integrity group where she works on simulations and measurements of high-speed interconnection links.

Stefaan Sercu was born in Ieper, Belgium, on February 6, 1969. He received the degree in electrical engineering from the University of Gent in 1992. From 1992 to 1998, he worked as a research assistant at the Department of Information Technology (INTEC) of the university of Gent. His research concentrated on the characterization and modeling of high-speed connectors and interconnections. In 1998 he joined FCI where he is currently responsible for high-speed signal integrity simulations and measurements. In 2002 he received the PhD degree in electrical engineering from the University of Gent.

Dana J. Bergey was born in Lansdale, PA, on November 19, 1963. He earned his BS degree in Physics from the Pennsylvania State University, and his MSEE from the Air Force Institute of Technology. He spent several years working on stealth technology and teaching microwave and electromagnetics classes in the Air Force. He has spent the last 15 years working as a signal integrity and EMC engineer at AMP Incorporated, W.L. Gore & Associates, and FCI. Dana is presently manager of FCI's US signal integrity team, which is involved in the development of next-generation high-speed interconnects.

1. Introduction

When designing high speed systems, hardware designers have multiple options available to maximize system performance by optimizing each component within their design: transmitters and receivers (with or without signal conditioning), standard or low loss PCB and cable materials, standard open-pin-field connectors or high-speed connectors with matched impedance, low cross-talk and fixed signal/ground configuration. In recent years, each of these components of a link has been addressed. Once new technologies were applied to solve a specific speed barrier, the focus shifted towards the next obstacle to higher-speed transmission. Today, a primary barrier to increasing data rates is the transition between connectors and PCBs, or the connector footprint. SMT connectors can enable a lot of flexibility in optimizing the performance of the connector to PCB transition, thereby breaking through this latest speed barrier. However, very little is known about when footprint optimization is required and how to optimize footprint performance. In this paper, these two questions are addressed.

The paper consists of two sections. The first section discusses how to optimize the performance (impedance, cross-talk, insertion loss) of surface mount (SMT) connector footprints. It is not the intention of the paper to repeat the conclusion that the performance of connector via holes is limited by the via hole stubs and that back-drilling or sequential lamination can solve this. It is however our intention to look at the specific design parameters of the footprint for SMT connectors. Examples of such parameters are the relative position of signal and ground via holes, the size of the drilled holes, the size of the pads, etc. The paper reviews multiple options of positioning via holes with respect to the SMT pads in order to optimize electrical performance, as well as routing density, creating a cost advantage by eliminating layers in the PCB. This first section applies to all applications that use high-speed, high-density SMT connectors (SATA, SAS, DDR, PCI-Express, backplane, etc.). The second part of the paper focuses on the performance benefit on a system level. By comparing the performance of real world applications that use press-fit connectors with the same applications using SMT connectors, the significance of the use of SMT connectors will be illustrated. Simulation and optimization of a connector footprint requires a fast and accurate simulation tool to be able to run a large number of configurations in a limited amount of time and with limited resources. The footprints in this paper are simulated using a dedicated in-house software tool that allows for fast and accurate simulation as opposed to a 3D full-wave simulation tool. The accuracy of the results obtained with this tool has already been demonstrated in previous publications [1-4].

2. Press-fit connector footprint performance

In this section the performance of the footprint of a traditional press-fit connector is studied. In the case of press-fit connectors, the footprint is almost completely determined by the selected connector and by its design. The diameter of the plated-through holes is determined by the size of the press-fit pins on the connector. Currently standard finished via hole diameters for press-fit connectors are about 0.5 to 0.6 mm. The column and row pitch of the connector determine the relative position in the footprint of the individual holes with respect to each other. Furthermore, most high-speed connectors that are available today have pre-defined ground and signal pins. The signal/ground configuration in the footprint must correspond to the signal/ground configuration in the connector. Once the connector is selected only a limited number of parameters of the footprint are available for further optimization.

2.1. Impact of the connector design on the footprint performance

Because the selection of the press-fit connector fixes most of the parameters of the footprint, selecting a different connector can initially optimize the performance of the footprint. In this section, we study the impact on the footprint performance of two parameters that are determined by the selection of the connector: 1) the signal/ground configuration and 2) the column pitch. As will be clear from the results shown in this section these parameters have a big impact on the footprint performance, especially the cross-talk performance. The decisions that are made when designing a

connector will impact the performance of the footprint of the connector and hence, the overall performance of the transition from one board to another. These decisions have to be made carefully so that the footprint does not degrade performance too much.

2.1.1. Impact of the signal/ground configuration

High-speed connectors usually have a fixed signal/ground configuration. The assignment of signals and grounds to the connector pins is pre-determined for optimal performance. In the case of a press-fit connector the signal/ground configuration of the footprint is the same as that of the connector. If the selected connector is an open-pin-field connector, the signal/ground configuration can still be chosen arbitrarily and optimized for best performance.

The applied signal/ground configuration will have a big impact on the cross-talk performance of the footprint (and of the connector). Figure 1 shows two possible configurations for assigning 4 differential pairs. The signal pins can be arranged on a square grid, meaning there is no offset between the location of the signal pins in adjacent columns (figure 1a), or they can be staggered, meaning there is an offset S between adjacent columns (figure 1b).

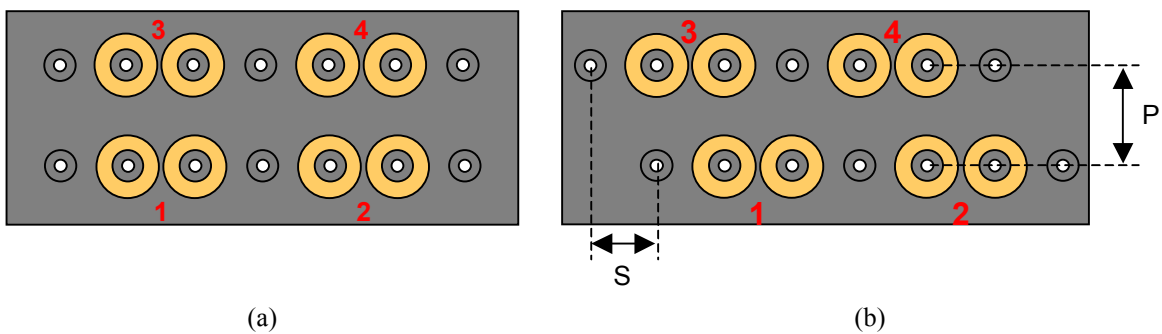


Figure 1: Signal/ground configuration: square grid (a) vs. staggered grid (b).

The board build-up used in the simulations is shown in figure 2. The board material is FR4, with a dielectric constant of 3.5 and a loss tangent of 0.02. The board consists of 8 layers. The total thickness is about 3.2 mm, and the traces are routed on the bottom signal layer. The same board build-up will be used for all analyses presented in this paper. Figure 3 shows the cross-talk between the differential pairs for a square via field and for a staggered via field, and for a 2 mm and a 3 mm column pitch (P in figure 1b). The offset S between two adjacent columns in the staggered footprint is 1.4 mm, which is equal to the pitch of the vias within the columns. The holes have a drilled diameter of 0.6 mm and the pad and anti-pad diameters are 0.9 and 1.4 mm respectively. The dashed lines in figure 3 represent the cross-talk in the square footprint, and the solid lines represent the cross-talk in the staggered footprint. The red numbers in figure 1 depict the definition of the differential pairs. Clearly the cross-talk in the case of a staggered footprint is significantly lower than that in the case of a square footprint.

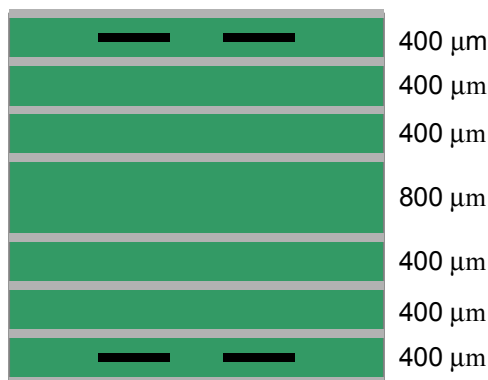


Figure 2: Board build-up used in via simulations

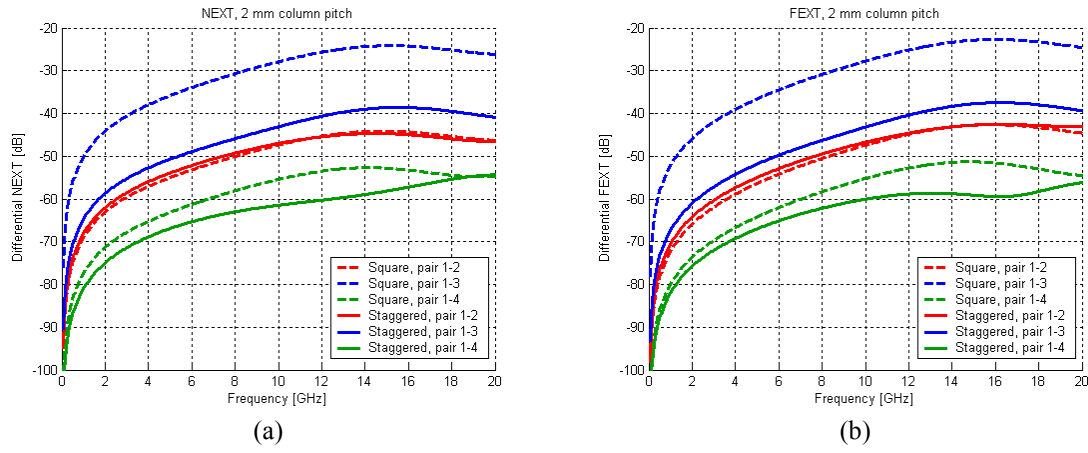


Figure 3: Pair-to-pair cross-talk for a square and a staggered grid: (a) NEXT and (b) FEXT.

One can optimize the offset S between two adjacent columns to minimize the multi-line cross-talk. In this case, the multi-line cross-talk is defined as the worst-case cross-talk on a victim pair caused by 8 neighboring aggressor pairs (figure 4a). Figure 4b shows the multi-line cross-talk as a function of the offset between columns for a 2 mm column pitch. From this figure, the optimal offset can be determined. If one assumes that the optimal offset is that for which the multi-line NEXT and FEXT are minimized, then the optimal offset is about 1.2 mm. This corresponds to a minimum NEXT and FEXT at 25 ps (10-90 % rise time) of about 1.2 %. In case of a square grid the NEXT and FEXT are 4.0 and 4.2 % respectively.

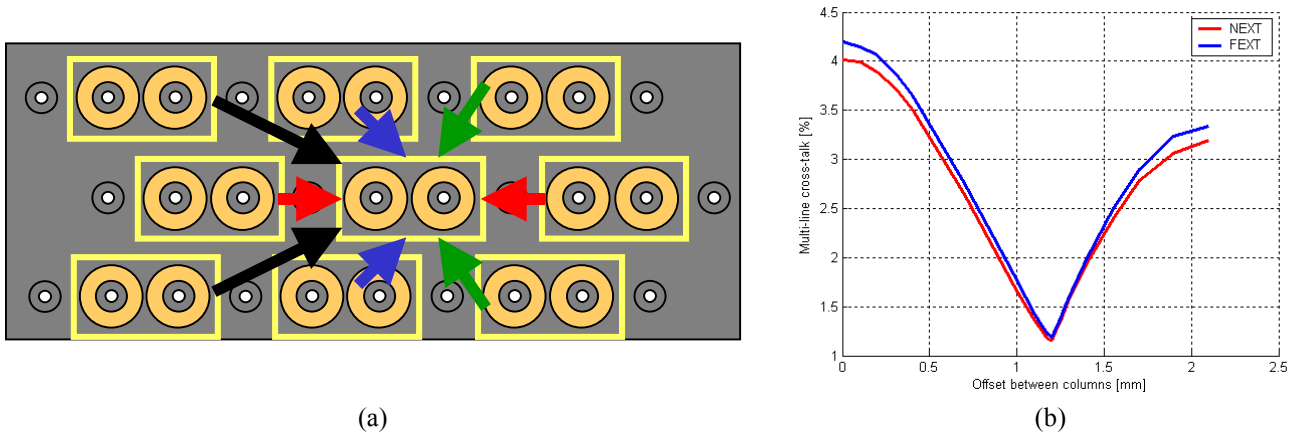


Figure 4: (a) Multi-line cross-talk definition, (b) multi-line cross-talk as a function of the offset between columns for a 2 mm column pitch.

One can conclude that a significant reduction of cross-talk in the footprint can be obtained if a connector with a staggered footprint is used.

2.1.2. Impact of the column pitch

The connector column pitch affects not only the footprint performance (column-to-column cross-talk) but also the available routing space (i.e. the available space between the vias for routing the differential pairs). Figure 5 shows that the available routing space is equal to the column pitch P minus the diameter of the anti-pad AP minus 2 times the misalignment MA between layers. As the column pitch increases, the available routing space increases as well. This additional routing space can be used either to route wider traces or to increase the number of differential pairs routed per column. The latter is very interesting because it allows one to reduce the number of signal layers, which makes the overall board thickness smaller. Preferably traces should not be routed in the area below the anti-pads since the absence of a ground plane above and below the signal tracks in this area could increase the cross-talk between traces routed on different layers. In addition, the matched impedance of the traces would be lost in this area.

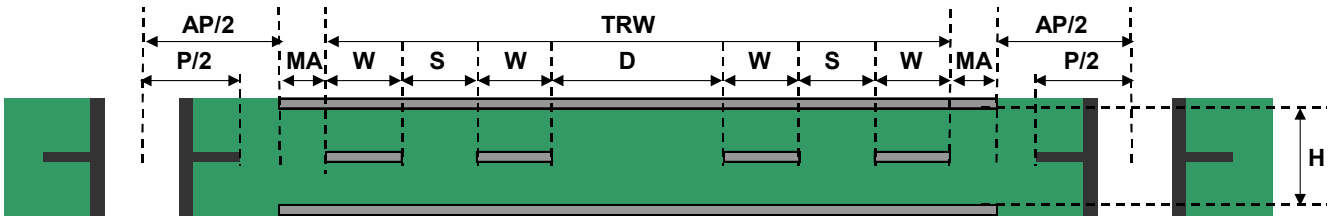


Figure 5: Definition of trace and via hole parameters.

2.1.3. Trace width

Wider traces are beneficial because the losses decrease when the trace width increases. Figure 6a shows the differential insertion loss at 5 GHz of edge-coupled striplines for different trace lengths. Figure 6b shows the gain that can be achieved by making the trace width larger than 100 μm . It is clear that for short traces only a limited improvement in loss can be achieved. If the trace length is only 10 cm, then 0.6 dB gain is achieved when the trace width is increased from 100 μm to 300 μm . Furthermore it is also clear that most reduction in losses can be achieved in the 100-200 μm region. If the trace length is 0.5 m, then a reduction by more than 2 dB is achieved by increasing the trace width from 100 μm to 200 μm . But if the trace width is increased further to 300 μm , the additional gain is less than 1 dB.

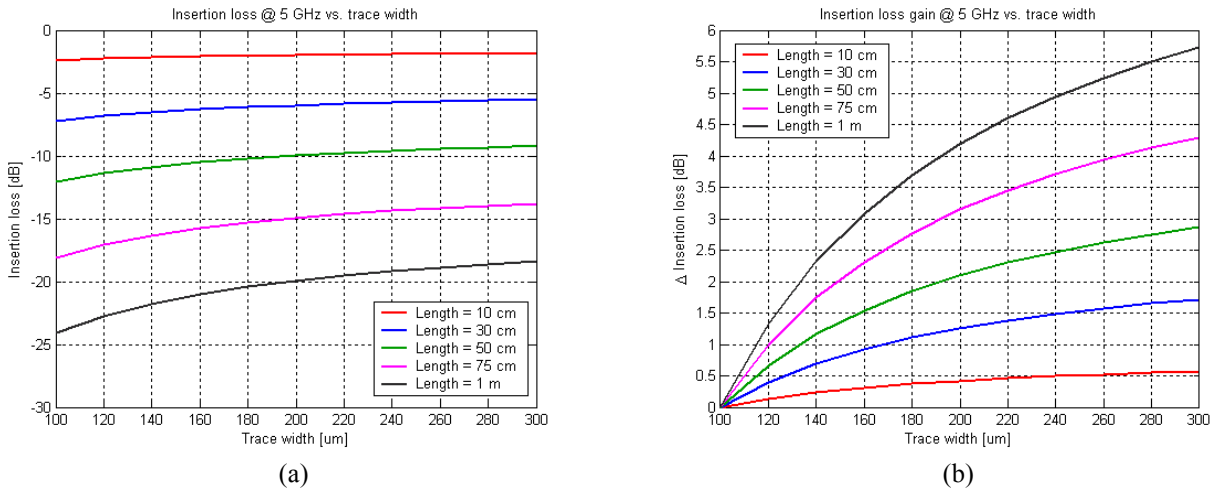


Figure 6: (a) Insertion loss of differential edge coupled striplines vs. trace width, (b) insertion loss gain made when traces are wider than 100 μm .

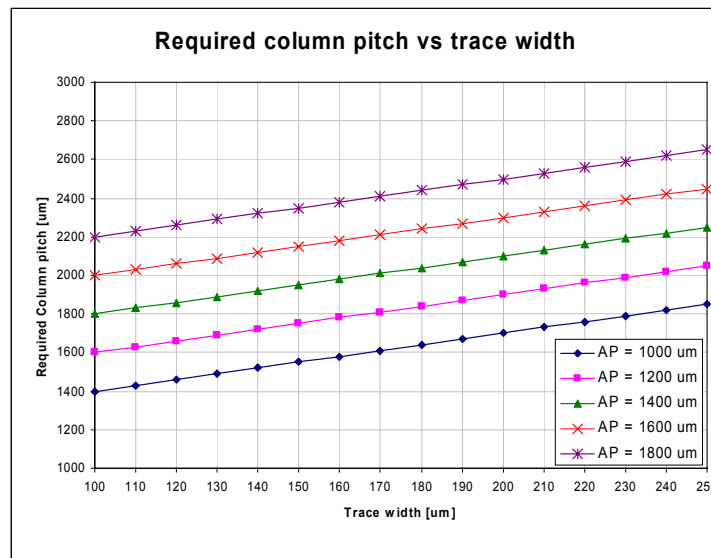


Figure 7: Minimum-required column pitch for a given trace width.

Figure 7 shows the relationship between the minimum-required column pitch and the trace width for different anti-pad diameters. It is assumed that the isolation S within a differential pair is identical to the trace width W , and that the distance MA between the edge of the signal trace and the edge of the ground plane is $50\ \mu\text{m}$. It is clear that in order to use wider traces, the column pitch must be wide enough to avoid having to reduce the anti-pad diameter. It also needs to be noted that in order to maintain the required impedance, increasing the trace width requires thicker board substrates. If this is not acceptable, an alternative can be to increase the space between traces. This latter might also require a larger column pitch.

2.1.4. Double density routing

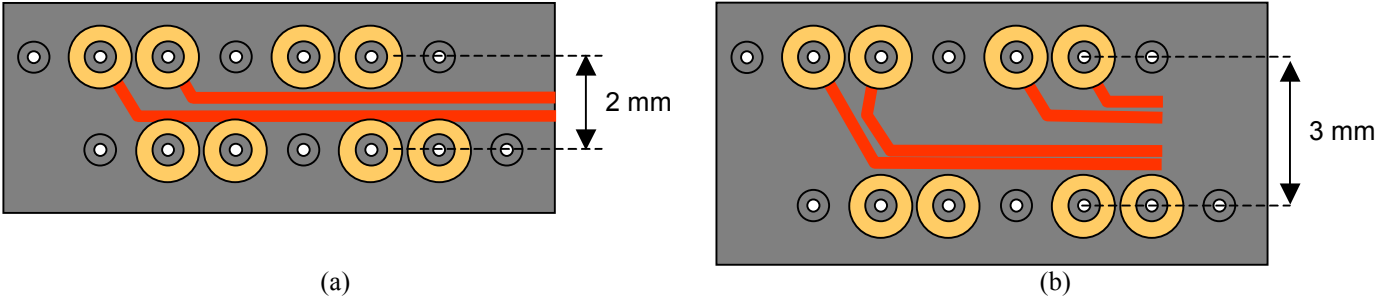


Figure 8: (a) Single density routing vs. (b) double density routing.

Instead of using the additional routing space for increasing the routing width, it can also be used to increase the number of differential pairs that is routed per column as shown in figure 8. If the column pitch is large enough to allow two (or even more) differential pairs to be routed per column, then the total number of layers in the PCB and consequently the overall PCB cost can be minimized. The space needed for routing multiple differential pairs is determined by the trace width and by the intra-pair and inter-pair spacings. The spacing between two adjacent differential pairs must be sufficiently large to minimize the cross-talk between the two pairs. Figure 9 shows the pair to pair near-end (a) and far-end (b) cross-talk as a function of the isolation between the pairs (10-90 % rise time = 25 ps). Results are shown for different coupling lengths. Figure 10 shows the dimensions of the PCB structure. It is clear from the figures that, if saturated, near-end cross-talk is significantly larger than far-end cross-talk and that near-end cross-talk is independent of the length of the traces. If we assume the pair-to-pair near-end cross-talk must be smaller than 0.5 %, then the pair-to-pair isolation must be at least $500\ \mu\text{m}$. This corresponds to 2.5 times the intra-pair isolation S .

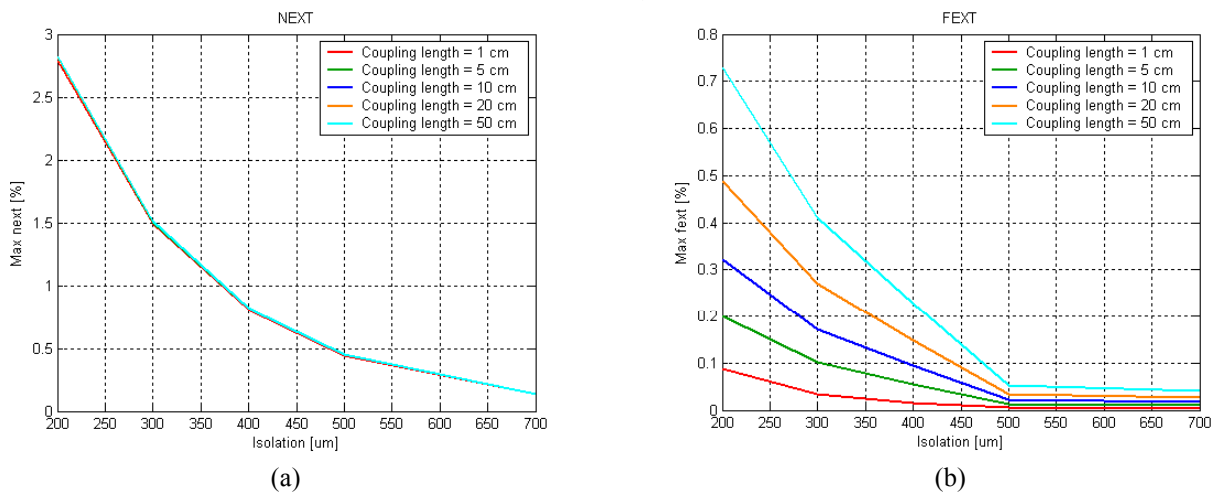


Figure 9: (a) Pair-to-pair near-end and (b) far-end cross-talk between two differential traces as a function of the distance D between pairs, for different coupling lengths.

Figure 11 shows the required column pitch when multiple pairs are routed per column. To minimize cross-talk between differential pairs it was assumed that the isolation D between pairs was equal to 3 times the intra-pair spacing S . Furthermore it was assumed that the intra-pair spacing was equal to

the trace width W . The anti-pad diameter was $1300\ \mu\text{m}$. From the figure one can conclude that if one wants to route two pairs with a trace width of $200\ \mu\text{m}$ within one column with less than 0.5% near-end cross-talk between the pairs, then the column pitch must be $3\ \text{mm}$. Furthermore notice that if the column pitch is $3\ \text{mm}$, then three pairs with a trace width of $120\ \mu\text{m}$ can be routed.

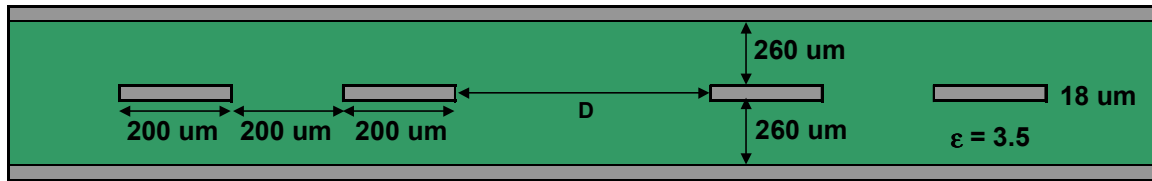


Figure 10: PCB build up for the pair-to-pair cross-talk study

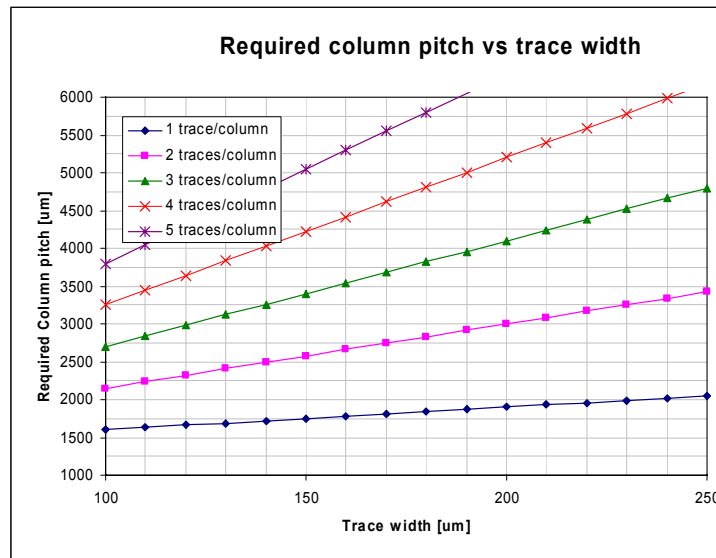


Figure 11: Required column pitch as a function of the trace width for routing multiple pairs per column, $AP = 1300\ \mu\text{m}$.

2.2. Additional optimization of the press-fit footprint

Once the connector is selected, and the hole diameter and signal/ground configuration are determined, a number of parameters remain that can be optimized to maximize the footprint performance. These parameters are the via pad size, the via anti-pad size and shape, the via stub-length and the routing. These parameters can be optimized within the boundaries determined by the limitations inherent in board manufacturability.

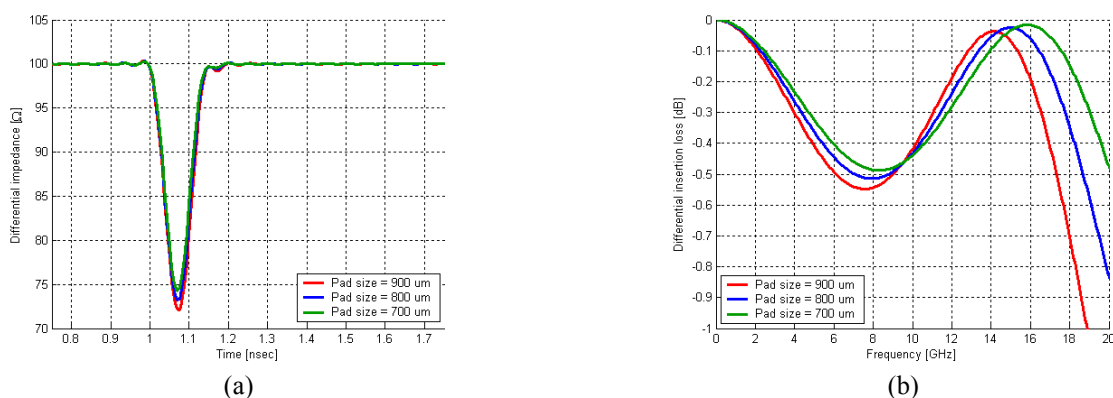


Figure 12: (a) Impact of the via pad size on the differential impedance (for a 10-90 % rise time of 50 ps) and (b) on the differential insertion loss.

Reducing *the pad size* reduces the capacitance of the via hole and consequently increases the impedance. Assuming that a via generally exhibits a capacitive behavior, this reduces the return and insertion losses of the via hole, thus improving performance. Figure 12 shows the impact of the via

pad size on the differential impedance (for a 10-90 % rise time of 50 ps) and on the differential insertion loss. The diameter of the antipads is 1.4 mm. Reducing the pad size results in only limited improvement. The impedance increases only by about $2\ \Omega$ at 50 ps, and the insertion loss improves by about 0.1 dB at 5 GHz.

A second parameter that can be optimized is *the anti-pad size*. Figure 13 shows the impact of the anti-pad diameter on the insertion loss (a) and impedance (b) for the via hole structure shown in figure 14. There is a significant decrease in insertion loss of 0.6 dB at 5 GHz when the anti-pad increases from 1000 μm up to 1400 μm . Further increase of the anti-pad diameter shows only a limited improvement of the insertion loss performance (0.2 dB if the anti-pad increases from 1400 μm up to 2400 μm). The same conclusion can be drawn for the impedance. If the anti-pad diameter increases from 1000 μm up to 1400 μm , the via hole impedance increases from 55 Ω up to 70 Ω . An additional impedance increase of 5 Ω can be obtained if the anti-pad is further increased to 2400 μm .

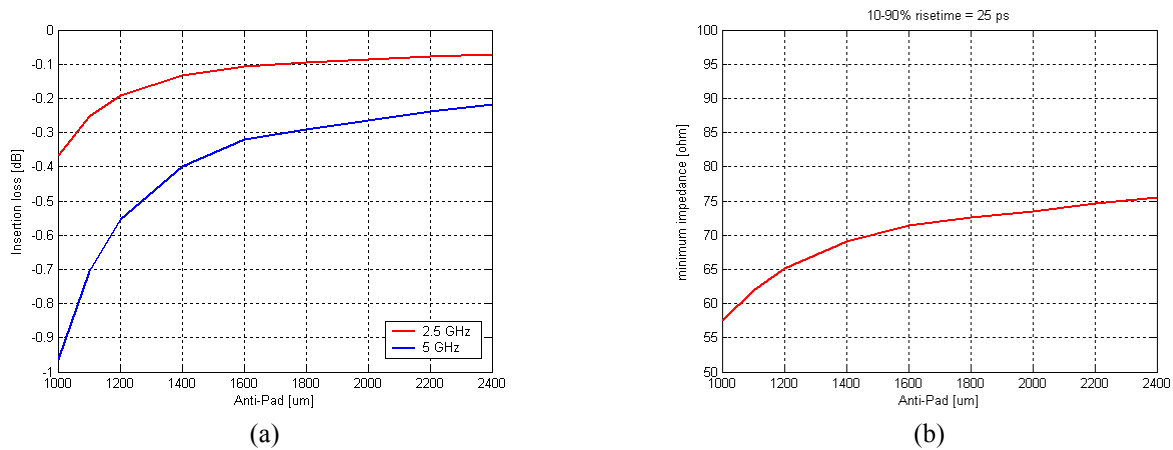


Figure 13: Impact of the anti-pad diameter on (a) differential insertion loss and (b) impedance.

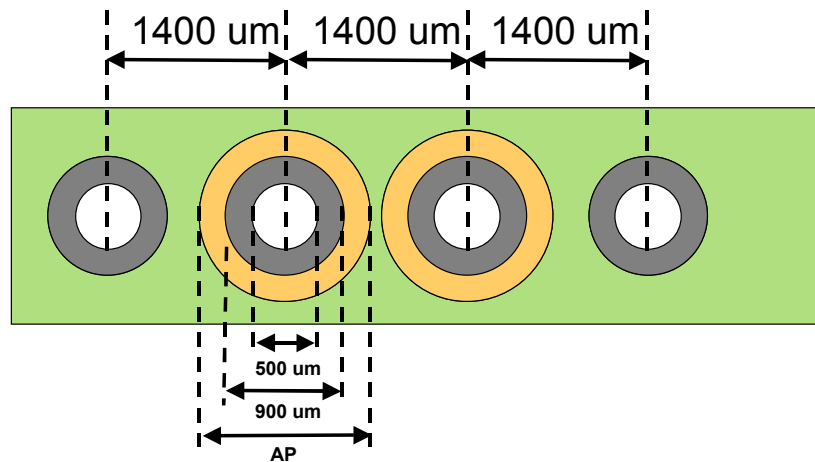


Figure 14: Definition of via hole parameters

One must also be aware that increasing the anti-pad implies that the ground planes above and below signal traces routed through the via field are removed locally. The impedance of these traces will increase locally and also the cross-talk between traces routed on different layers will increase because of the removal of the ground planes between them. Therefore, in practice, the size of the anti-pads should be limited by the routing width augmented with the layer misalignment and vice-versa.

Long via stubs cause a resonance dip in the insertion loss profile and deteriorate the performance of the via dramatically. Back-drilling is a well-established technique for reducing or removing the via stub and is common practice in high-speed printed circuit boards. For the remainder of this paper it is assumed that all via holes have minimal stub length, implying that they are back-drilled when necessary.

Finally, *the routing* will also determine the performance of the footprint. Signals routed on the top signal layer will result in vias that have a large stub-length and may require back-drilling (introducing an additional cost for the PCB manufacturing), while vias connecting traces routed on the bottom layer may not require back-drilling but will have an increased cross-talk because of the larger barrel length resulting in longer coupling lengths. Routing more differential pairs on the same layer will enable to reduce the overall layer count and reduce the total cost of the PCB. However if the column pitch is maintained, this will reduce the trace width and will therefore increase the trace losses.

2.3. Recommendations

To conclude this section a number of recommendations for press-fit connector footprints can be formulated. First, using a staggered footprint can yield a significant cross-talk reduction.

If a via hole for a press-fit pin with a drilled hole size of 600 μm (finished hole size = 500 μm) needs to be designed then the anti-pad should be between 1200 μm and 1600 μm . Larger anti-pads limit the available space for routing and do not significantly increase performance.

Double-density routing allows a reduction in the overall layer count and thus in the cost of a PCB. If, in order to transmit at higher speeds and/or across longer lengths, traces with a width of 200 μm are required, then the via hole column pitch should be at least 3 mm to enable double-density routing.

3. SMT connector footprint performance

In the case of a SMT connector the design of the footprint can be (completely) separated from the design of the connector, enabling a lot more freedom to optimize the connector footprint. There are two major benefits of having a SMT connector. First, the drilled hole size can be reduced. The reduced hole size increases the available routing width, which again can be used to route wider traces or to route 2 or more differential pairs per column. Second, the relative position of the signal and ground vias within the footprint can be optimized for maximum performance (cross-talk, impedance, routing, etc.).

In this section it is the intention to study the footprint performance of two different connectors: AirMax VS[®] BGA on a 2 mm column pitch, and AirMax VS[®] BGA on a 3 mm column pitch. Figure 15 shows the footprint layout. The connector has a pre-defined signal/ground pin assignment. The footprint is staggered with a 1.3 mm offset between columns for optimal cross-talk performance.

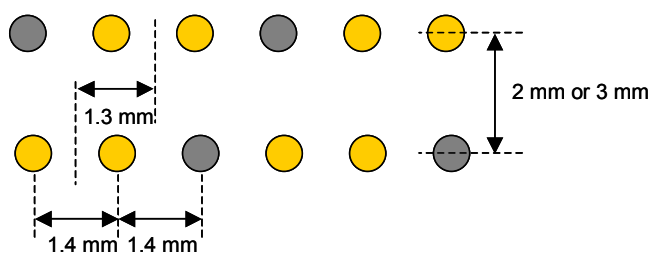


Figure 15: Footprint layout for the Airmax BGA connectors (2mm and 3 mm pitch).

3.1. Impact of the drilled hole size

For press-fit connectors the minimum size of the via holes is determined by the dimensions of the press-fit pins that must fit into the holes. For a BGA or SMT connector there is no press-fit pin, so the size of the via holes can be reduced. Smaller via holes will result in a better impedance and insertion loss and also yield additional routing space. The minimum size of the via holes is determined by limits in manufacturability. The minimum achievable ratio between the hole diameter and board thickness is limited by drilling and plating issues.

Figure 16 shows the impact of reducing the via hole size on the differential impedance (for a 10-90 % rise time of 50 ps) and on the differential insertion loss. The dotted lines represent a drilled hole size of 0.6 mm, i.e. a press-fit footprint, and the solid lines represent a drilled hole size of 0.4 mm, i.e. a SMT footprint. The offset between adjacent columns is 1.4 mm. The red lines are for a 2 mm

column pitch and the blue lines are for a 3 mm column pitch. By reducing the via hole size from 0.6 to 0.4 mm the differential impedance increases by about 20 Ω (to approximately 92 Ω), and the differential insertion loss is reduced to less than 0.05 dB at 5 GHz.

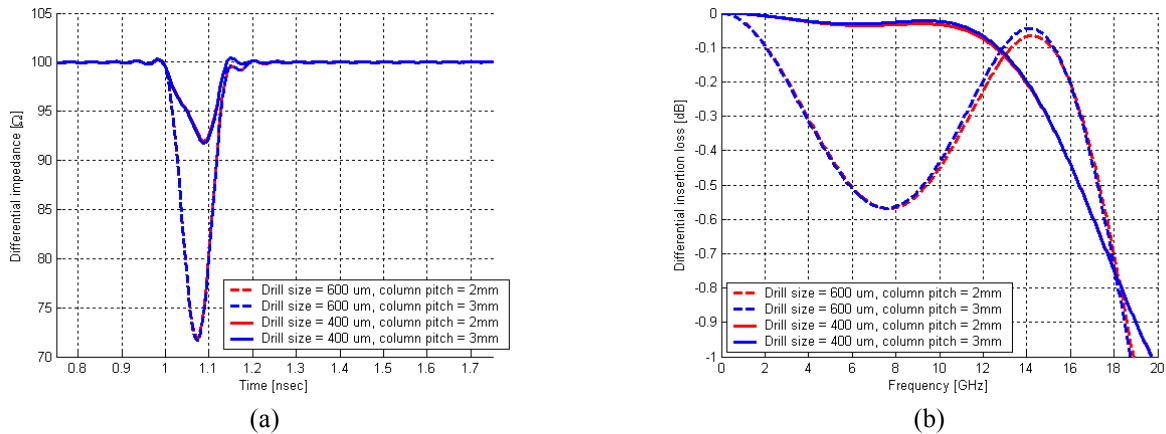


Figure 16: Impact of reducing the via hole size on (a) the differential impedance (for a 10-90 % rise time of 50 ps) and (b) on the differential insertion loss.

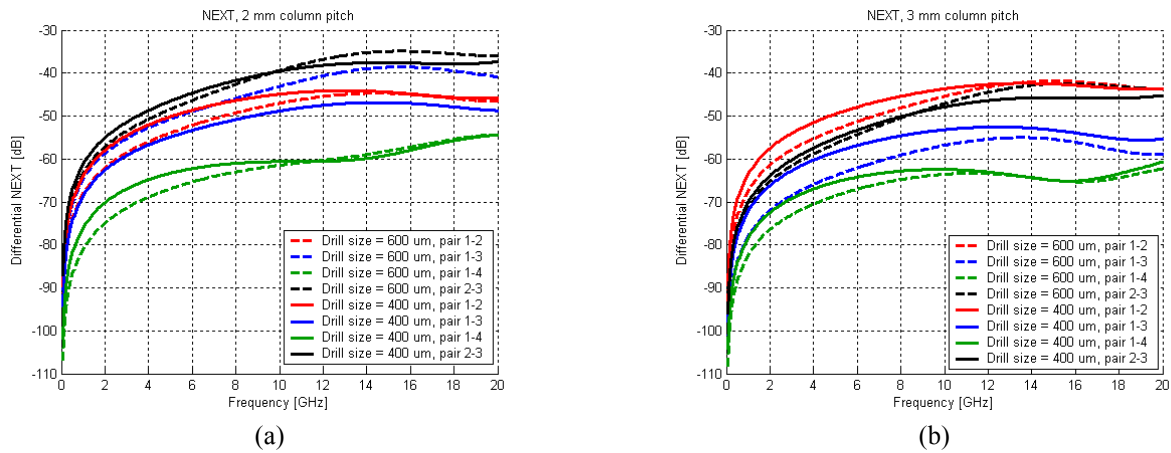


Figure 17: Impact of reducing the via hole size on the differential NEXT for (a) a 2 mm column pitch and for (b) a 3 mm column pitch.

Figure 17 shows the impact of reducing the via hole size on the differential NEXT for a 2 mm and a 3 mm column pitch. The definition of the differential pairs is shown in figure 1b. The colors used in figure 17 correspond to the colors of the arrows shown in figure 4a. Again, the dotted lines represent a drilled hole size of 0.6 mm, and the solid lines represent a drilled hole size of 0.4 mm. These figures show that the cross-talk may increase or decrease when the via hole size is reduced. In case of a 2 mm column pitch the cross-talk between pairs 1 and 3 decreases, in case of a 3 mm column pitch this cross-talk increases with decreasing via hole size.

3.2. Optimizing the relative position of the vias within the footprint

For BGA connectors the position of the via holes does not need to correspond to the position of the solder balls in the array. The solder pads used for terminating the connector to the board can be connected to the pads of the via holes using so-called ‘dogbones’. This way the position of the connector terminations and the vias in the footprint can be separated. The position of the via holes can be selected independently of that in the connector, both in the *column* direction (*x-direction*) and in the *row* direction (*y-direction*), and can be optimized for several performance measures like impedance, cross-talk, routing width and routing density. It will become clear from the following sections in general it will not be possible to find a common footprint for which all performance measures are optimal. Instead of trying to achieve the absolute optimum for all performance measures, a trade off will have to be made so that a single footprint is found with reasonable values for all performance measures.

3.2.1. Optimizing a single pair for minimum impedance variation and insertion loss

In this section a single differential pair consisting of two signal vias flanked by two ground vias is optimized for minimum impedance variation by positioning the vias relative to the ground vias and to each other. Figure 18a shows the geometry and the optimization parameters. The drilled hole diameter is fixed at 0.4 mm, the pad diameter is 0.7 mm and the antipad diameter is 1.4 mm. Three performance measures are taken into account: the impedance (for a 10-90 % rise time of 50 ps) and the insertion loss at 5 and 10 GHz. The performance measure for the impedance is defined as

$$dZ = -\sqrt{(Z_{\max} - 100)^2 + (Z_{\min} - 100)^2}$$

where Z_{\max} and Z_{\min} are the maximum and minimum value in the time domain impedance profile.

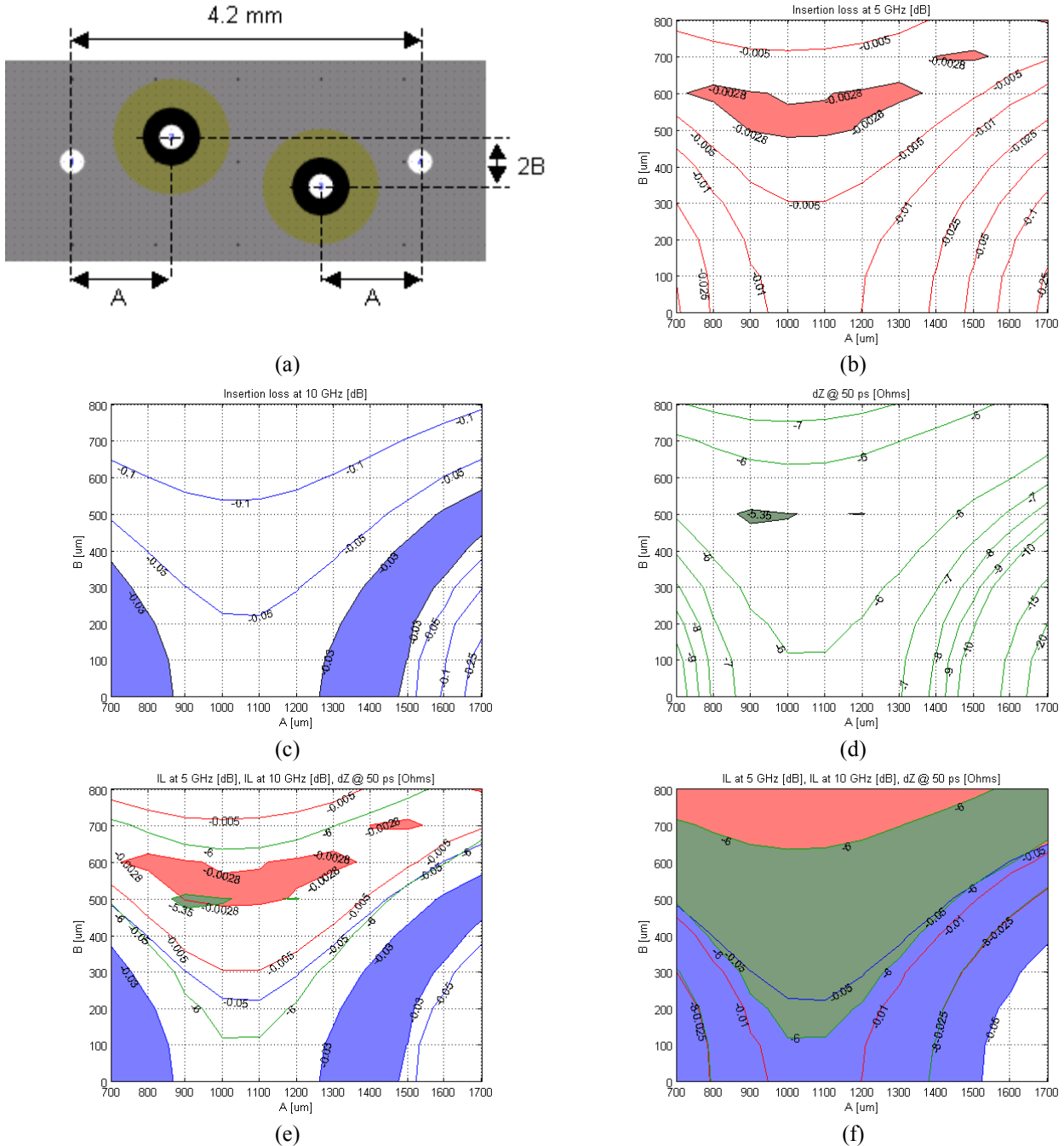


Figure 18: Optimization of a single differential pair: (a) geometry and optimization parameters, contour plot of the insertion loss at (b) 5 GHz and at (c) 10 GHz, (d) contour plot of dZ , (e) optimum regions for the insertion loss and the impedance, (f) regions where the insertion loss at 5 GHz is better than 0.01 dB, the insertion loss at 10 GHz is better than 0.05 dB and $|dZ|$ is better than 6.

Figure 18b shows a contour plot of the insertion loss at 5 GHz. The filled region corresponds to the area of minimum insertion loss, which is about -0.003 dB. Figure 18c shows a contour plot of the insertion loss at 10 GHz. The minimum insertion loss at 10 GHz is about -0.03 dB. Figure 18d shows a contour plot of dZ . In figure 18e the three performance measures are combined into a single plot. The three performance measures do not reach their optimum for the same values of A and B . The insertion loss at 5 GHz and dZ both reach their optimum value for $A = 900 \mu\text{m}$ and $B = 500 \mu\text{m}$, but in that case the insertion loss at 10 GHz is not optimal. Figure 18f shows the regions where the insertion loss at 5 GHz is better than 0.01 dB, the insertion loss at 10 GHz is better than 0.05 dB and $|dZ|$ is better than 6Ω ($Z \approx 100 \Omega \pm 5 \Omega$). A footprint that lies in the overlap region is the one for $A = 1100 \mu\text{m}$ and $B = 200 \mu\text{m}$.

Figure 19 shows the differential impedance and insertion loss for three different configurations. The red line represents the configuration with the vias in the press-fit position, the blue line represents the configuration with optimal impedance and insertion loss at 5 GHz, and the green line represents the configuration with combined optimized impedance and insertion loss at 5 and 10 GHz. Figure 20 shows the footprints corresponding to the results shown in figure 19.

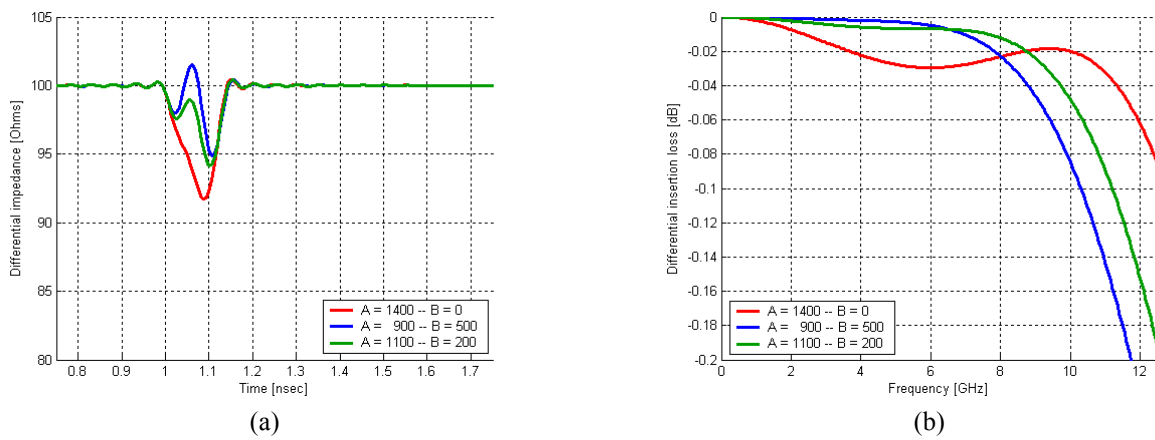


Figure 19: (a) Differential impedance and (b) insertion loss for the initial configuration (red line), the configuration with optimal impedance and insertion loss at 5 GHz (blue line) and the configuration with optimal combination of impedance and insertion loss at 5 and 10 GHz (green line).

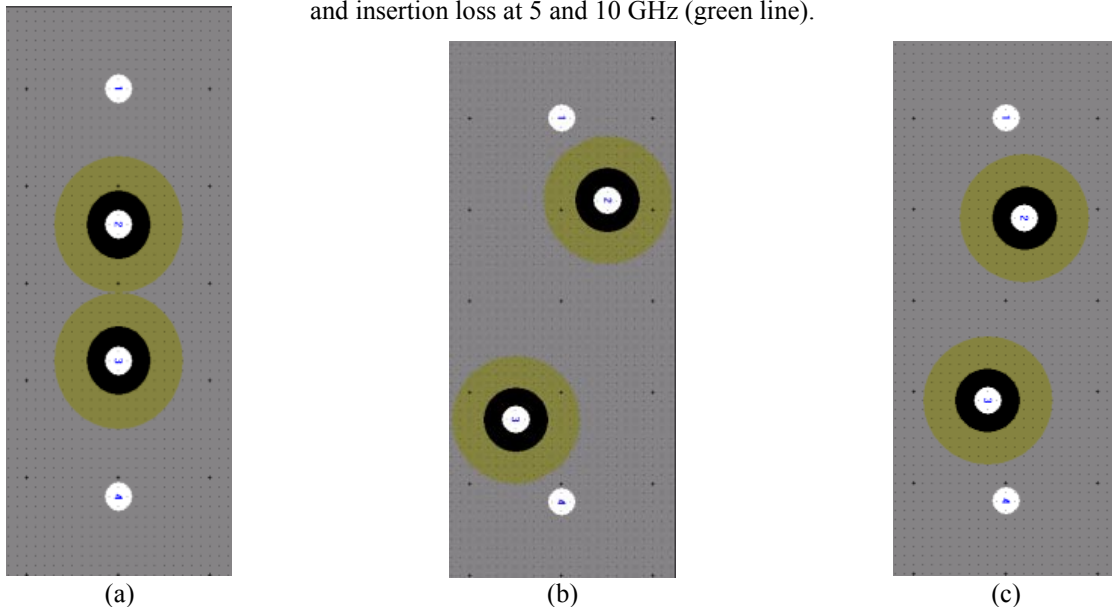


Figure 20: Footprints shown in figure 19: (a) $A = 1400$ and $B = 0$, (b) $A = 900$ and $B = 500$, (c) $A = 1100$ and $B = 200$.

3.2.2. Optimizing the footprint for cross-talk, impedance and insertion loss

For a column-to-column pitch of 2 mm the dominating cross-talk is that between differential pairs in adjacent columns. In this section the column-to-column cross-talk is optimized for a 2 mm and a 3 mm column pitch. Figure 21a shows the optimized geometry and the geometrical parameters. D is

the column pitch. Again, the drilled hole diameter is fixed at 0.4 mm, the via pad diameter is 0.7 mm and the anti-pad diameter is 1.4 mm. The offset between two adjacent columns is 1.4 mm. A is the translation of a via from the reference point in the y -direction, i.e. the vertical direction. Within a pair both via holes shift in opposite directions, (e.g. via 2 goes up and via 3 goes down.) A is identical for both pairs. B_1 and B_2 are the translation from the reference point in the x -direction, (i.e. the horizontal direction.) B_1 is the translation in the first differential pair, and B_2 is the translation in the second pair. Within a pair, both via holes shift in opposite directions, (e.g. via 2 goes right and via 3 goes left.) The horizontal shift in both pairs can be identical, $B_1 = B_2$, or it can be opposite, $B_1 = -B_2$. B_1 and B_2 are combined in a single geometrical parameter B . If B is positive, then $B_1 = B_2 = B$, and if B is negative, then $B_1 = -B_2 = |B|$.

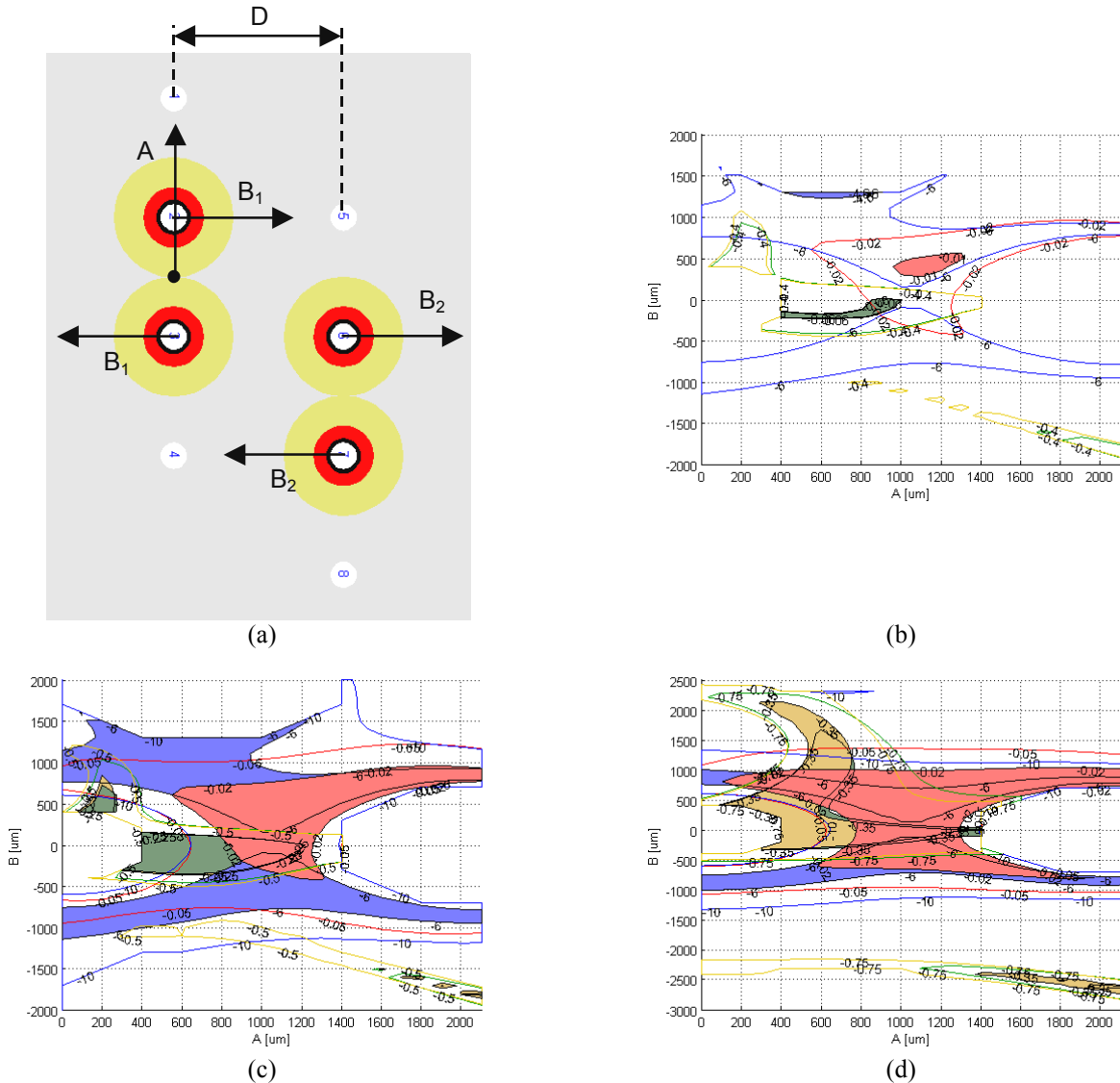


Figure 21: Optimization of the column-to-column cross-talk: (a) optimized geometry and the geometrical parameters, (b) areas of optimal insertion loss, dZ , NEXT and FEXT for a 2 mm column pitch, (c) areas of combined optimized insertion loss, dZ , NEXT and FEXT for a 2 mm column pitch, (d) areas of combined optimized insertion loss, dZ , NEXT and FEXT for a 3 mm column pitch.

Figure 21b shows the areas of optimal insertion loss at 5 GHz (0.01 dB, red area), optimal $|dZ|$ (4.6 Ω , blue area), optimal NEXT at 25 ps (0.06 %, green area) and optimal FEXT at 25 ps (0.06 %, yellow area) in the case of a 2 mm column pitch. There is no common footprint for which the insertion loss, impedance, NEXT and FEXT are all optimal. Figure 21c shows the regions where the insertion loss at 5 GHz is better than 0.02 dB (red area), $|dZ|$ is better than 6 Ω (blue area), and the NEXT and the FEXT at 25 ps are better than 0.25 % (green and yellow area respectively). In this case there are a number of footprints that satisfy these conditions. To maximize the available routing

space a footprint is chosen with $|B|$ as small as possible, i.e. $A = 1000 \mu\text{m}$, $B_1 = 100 \mu\text{m}$ and $B_2 = -100 \mu\text{m}$. This footprint is shown in figure 22a.

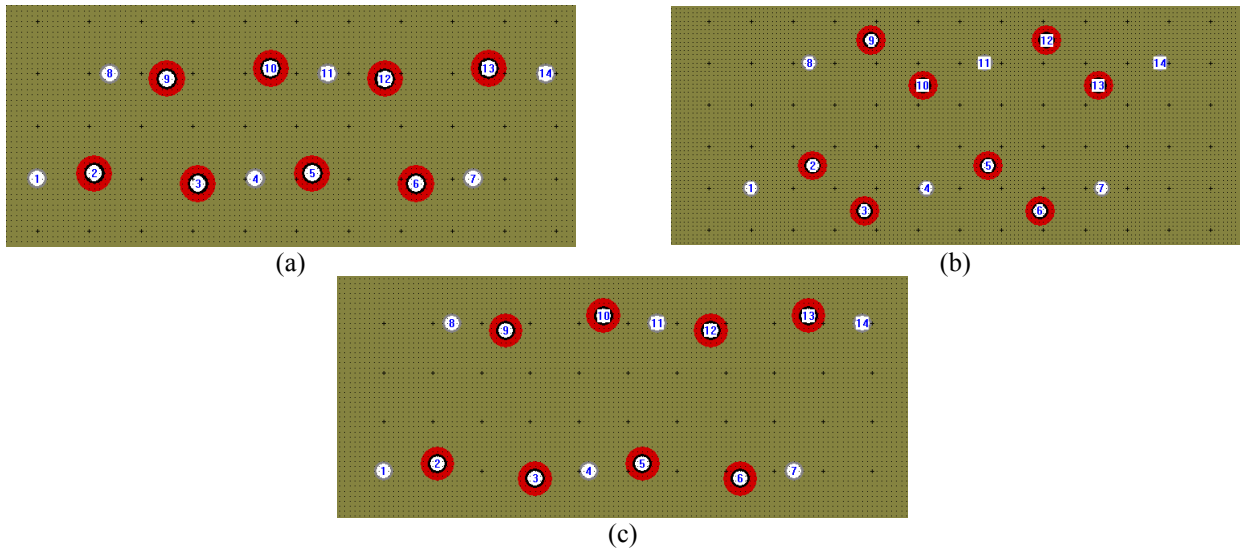


Figure 22: Footprints selected for optimal column-to-column cross-talk: (a) $A = 1000 \mu\text{m}$, $B_1 = 100 \mu\text{m}$ and $B_2 = -100 \mu\text{m}$, 2 mm column pitch, (b) $A = 620 \mu\text{m}$, $B_1 = 540 \mu\text{m}$ and $B_2 = 540 \mu\text{m}$, 3 mm column pitch, (c) $A = 1000 \mu\text{m}$, $B_1 = 150 \mu\text{m}$ and $B_2 = -150 \mu\text{m}$, 3 mm column pitch.

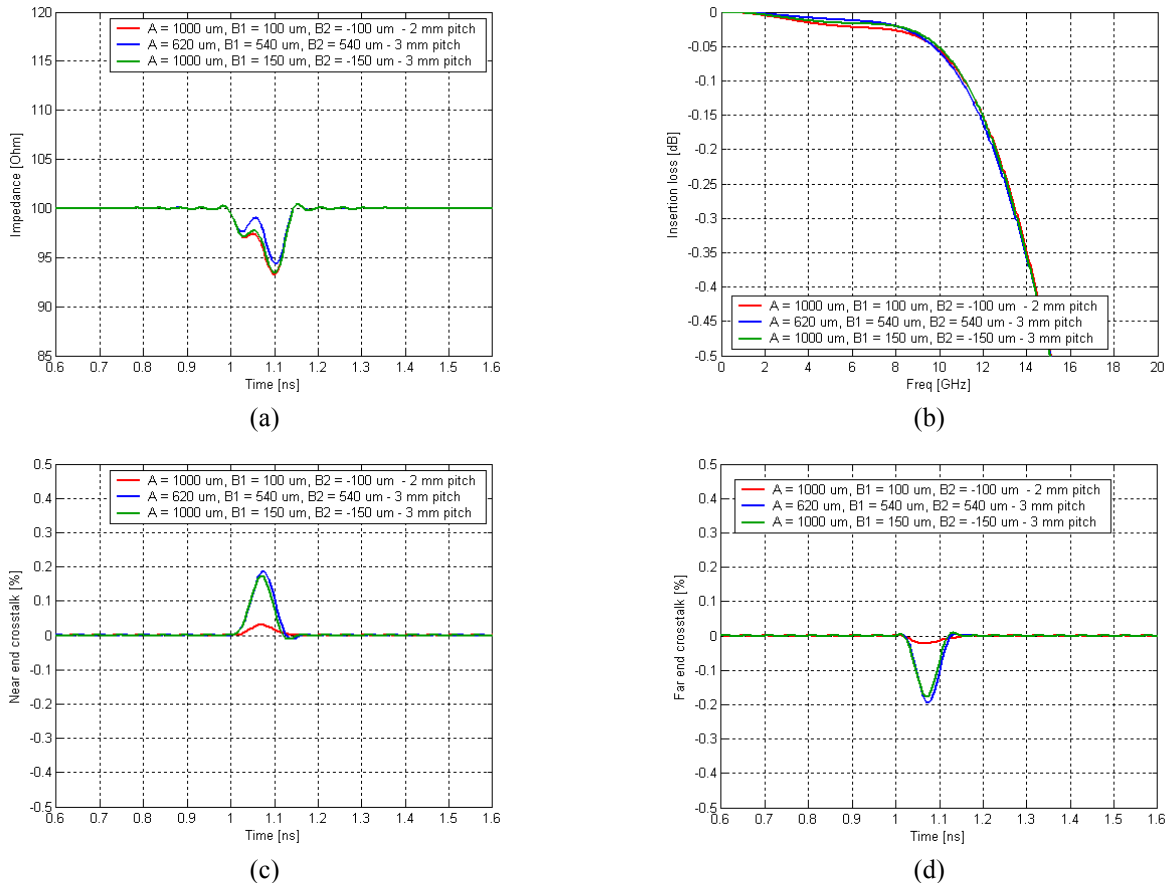


Figure 23: Signal integrity performance of footprints optimized for column-to-column cross-talk: (a) impedance, (b) insertion loss, (c) near-end cross-talk, and (d) far-end cross-talk.

Figure 21d shows the same as figure 21c, except now the column pitch is 3 mm instead of 2 mm, and the maximum NEXT and FEXT is 0.35 %. Again, there are a number of footprints that satisfy these conditions. Two footprints are selected, one for B positive and a second one for B negative. $|B|$ is chosen as small as possible again, to maximize the available routing space. The selected footprints

are $A = 620 \mu\text{m}$, $B_1 = 540 \mu\text{m}$ and $B_2 = 540 \mu\text{m}$, and $A = 1000 \mu\text{m}$, $B_1 = 150 \mu\text{m}$ and $B_2 = -150 \mu\text{m}$ (figures 22b and 22c). Figure 23 shows the impedance, insertion loss, and near-end and far-end cross-talk for the selected footprints. They all satisfy the pre-defined conditions.

3.2.3 Optimizing for routing

Increasing the column pitch increases the available routing space in a footprint. However, this decreases the signal density, (i.e. the number of signals per square cm). Alternatively, the routing space can also be increased by shifting and re-arranging the columns, while keeping the column pitch constant. This way the number of pairs that can be routed per column can be increased from 1 to 2, or more pairs per column. If one assumes that the required trace width is $200 \mu\text{m}$ and that the intra-pair spacing is equal to the trace width, then the required routing width for 1 pair is 0.6 mm . If one further assumes that the minimum pair-to-pair spacing is 0.5 mm then the required routing width for 2 pairs is 1.7 mm , and for 3 pairs it is 2.8 mm .

3.2.3.1. Optimizing for routing in the column-direction

Figure 24 a shows the routing space available between two columns on a 2 mm pitch. Figure 24b shows a footprint where 2 columns in the connector are reduced to a single column in the footprint: the connector via holes are now on a 4 mm pitch. Every two columns, the space initially taken by one column of vias becomes available for extra routing. In the footprint a ground pin is removed between two adjacent pairs and two ground pins in the connector are connected to the same ground via. Because a ground pin is removed the cross-talk between two adjacent pairs within the same column will increase. The insertion loss and impedance will be changed as well because of the re-arrangement of the via holes, and optimization of the position of the holes with respect to each other for optimum cross-talk, insertion loss and impedance is necessary.

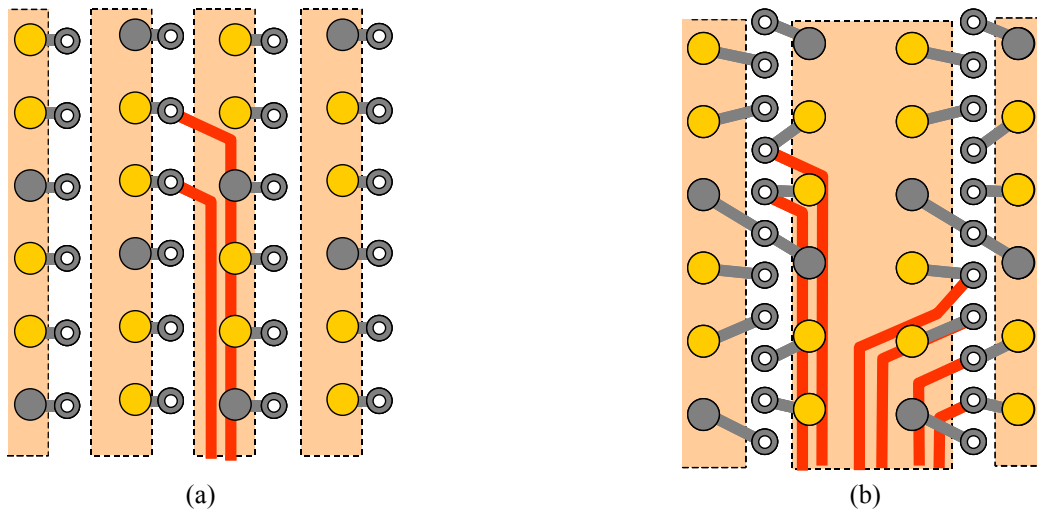


Figure 24: Available routing space: (a) standard footprint, (b) 2 columns reduced to a single column.

Figure 25a shows the optimized geometry and the geometrical parameters. X is the distance between two ground vias within a column and is equal to 4.2 mm , A is the distance from a ground via to the center of a differential pair, and B is the distance from the center of a via to the center of the via pair. Two different configurations are considered: a ‘standard’ configuration where the two differential pairs are separated (figure 25b) and an ‘interleaved’ configuration where one via of a differential pair is located between the two vias of the other differential pair (figure 25c). Figure 26 shows the NEXT, the FEXT, the impedance and the insertion loss for both configurations and for different values of A and B . The optimal configuration is the interleaved configuration with $A = 1600$ and $B = 900$. This configuration has optimal insertion loss, impedance and NEXT. The interleaved configurations have a much better impedance and insertion loss than the standard configurations. Of all interleaved configurations the one with $A = 1600$ and $B = 900$ has the lowest NEXT.

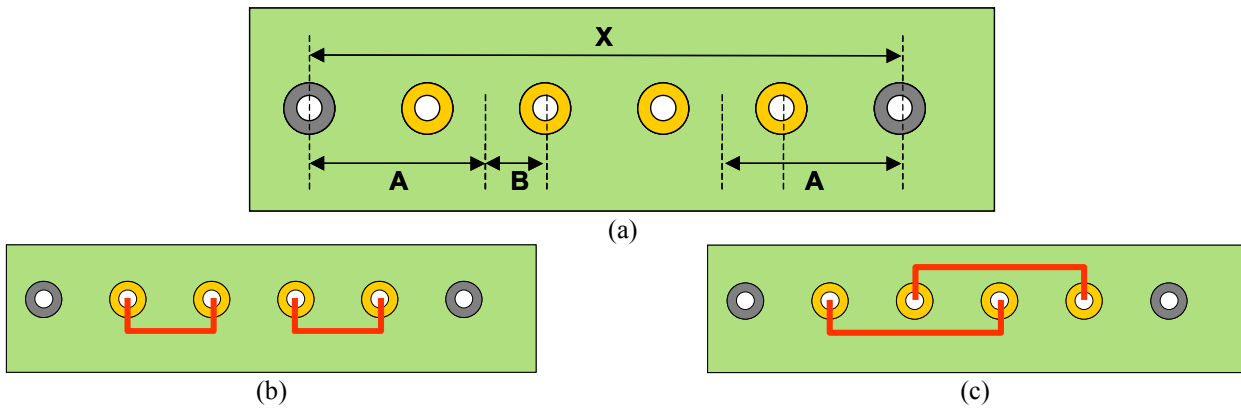


Figure 25: Optimization of two differential pairs flanked by two ground vias: (a) optimized geometry and the geometrical parameters, (b) 'standard' configuration and (c) 'interleaved' configuration.

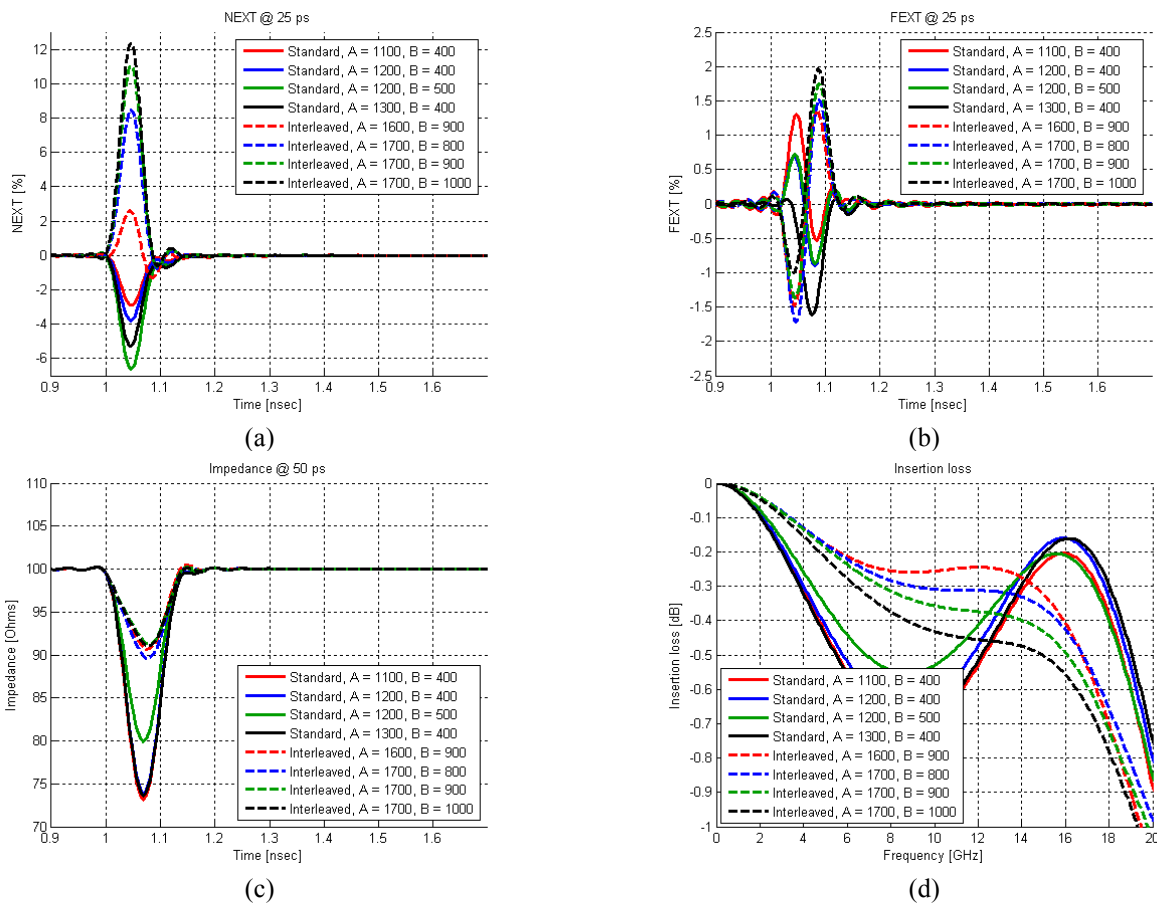


Figure 26: Optimization of two differential pairs flanked by two ground vias: (a) NEXT, (b) FEXT, (c) impedance and (d) insertion loss for both configurations and for different values of A and B .

3.2.3.2 Optimizing for routing in the column and row-direction

In addition to creating extra routing space in the x -direction, (i.e. between the columns,) extra routing space in the y -direction (between rows) can be created as well. Figure 27 shows two possible options. Both options allow to route not only in the x -direction but in the y -direction as well. Figure 27 (a) shows the options where the via holes of one differential pairs are brought closer together to minimize cross-talk. Figure 27 (b) shows the option where the impedance is optimized. Figure 28 shows the corresponding SI performance. The definition of the differential pairs is shown in figure 1b. The colors used for the cross-talk plot correspond to the colors of the arrows shown in figure 4a. The solid lines represent the results for the footprint with minimal cross-talk, the dotted lines represent the results of the footprint with the optimal impedance.

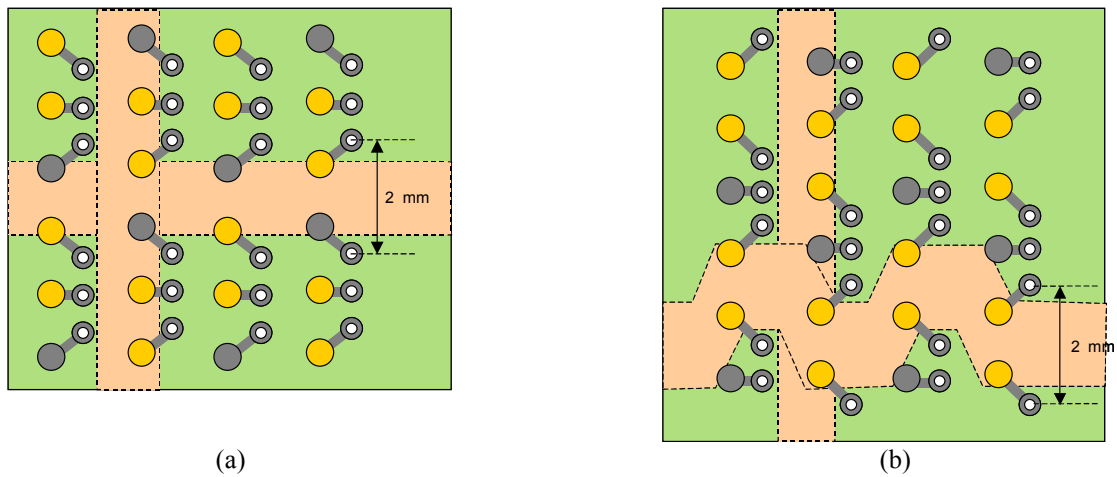


Figure 27: Options for optimizing the routing in the row directions: (a) minimizing cross-talk and (b) optimizing impedance.

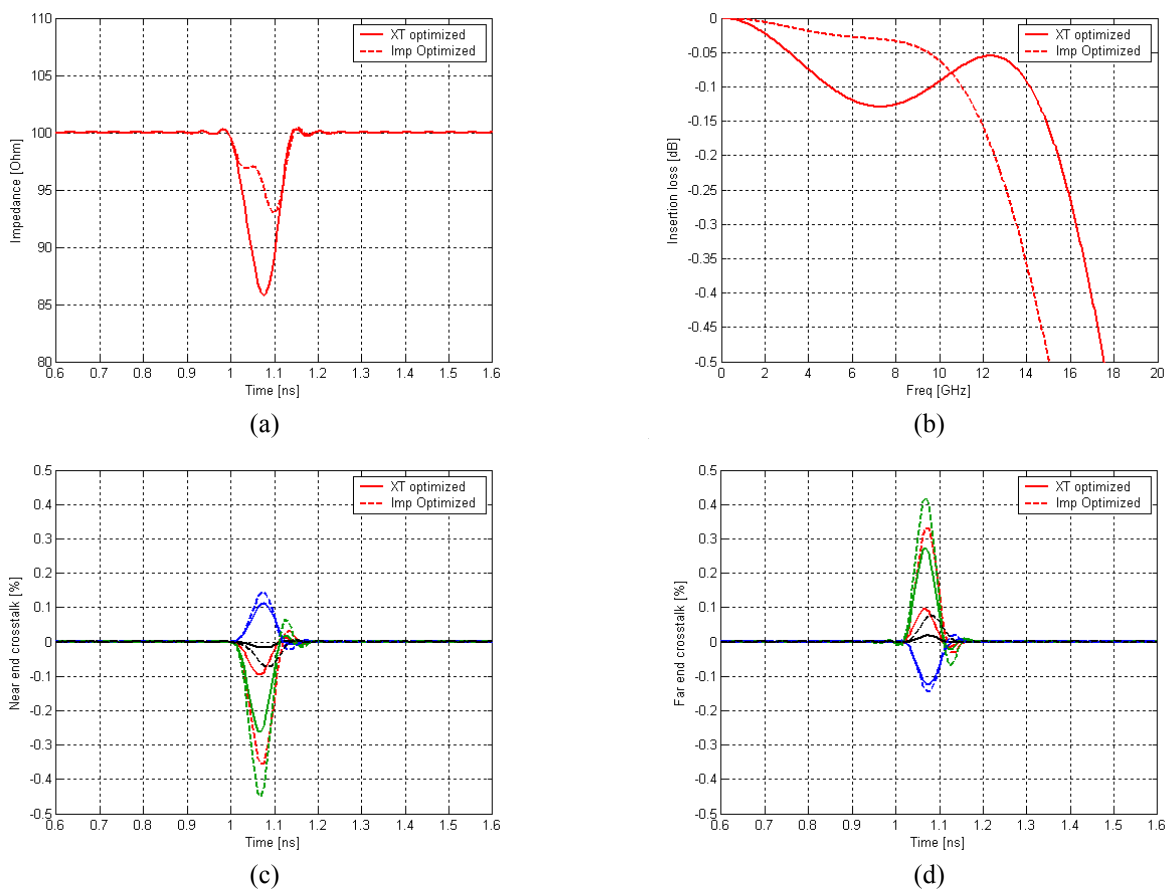


Figure 28: (a) Impedance, (b) insertion loss, (c) near-end and (d) far-end cross-talk of the footprints shown in figure 27. The color coding used for the cross-talk results is shown in figure 4.

Depending on which effect is more important: minimal cross-talk or optimal impedance, either footprint a or footprint b of figure 27 could be selected in an application that requires routing in both x- and y-direction.

3.3. Conclusions

From the previous sections it is clear that when it comes to optimizing the footprint there are a lot of possible options, and it is not always obvious which footprint is the most optimal. The different performance measures, including the insertion loss, impedance, near-end and far-end cross-talk and the routing, usually all have a different footprint for which they are optimal, and a trade-off has to be made between these performance measures. Since different applications have, in general, different

requirements with respect to the performance measures, every application can end up with a different optimal footprint.

4. Impact of different footprints on a link level

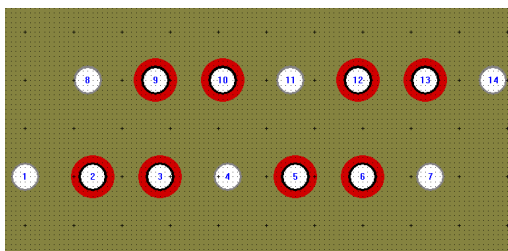
In this section the performance of a number of different footprints on a link level is compared. The link that is studied is the backplane link shown in figure 30. This link consists of a FR4 or Ro4350 backplane with two FR4 or Ro4350 daughter cards connected through two FCI AirMax VS[®] backplane connectors. Depending on the footprint considered, a press-fit version or a BGA version of the connector is used. The layer build-up of the backplane and the daughter cards is shown in figure 2. The traces on the daughter cards and on the backplane have a differential impedance of 100 Ω. Unless mentioned otherwise, the trace width is 200 μm, and the trace thickness is 18 μm. The board material is a “modified” FR4, with a dielectric constant of 3.5 and a loss tangent of 0.018, or Ro4350, with a dielectric constant of 3.5 and a loss tangent of 0.005. The length of the traces on the daughter cards is 5 cm. The backplane length *L* is variable. To minimize the impact of the via hole stubs, all traces are routed on the bottom signal layer. To allow the investigation of the impact of cross-talk, there are 4 differential pairs considered in the link. The pin assignment in both connectors is shown in table 1.

	Connector 1		Connector 2
Pair 1	D3-E3	connected to	G3-H3
Pair 2	G3-H3		D3-E3
Pair 3	E4-F4		H4-I4
Pair 4	H4-I4		E4-F4

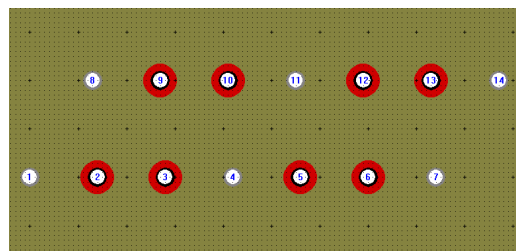
Table 1: Connector pin assignment.

The footprints on the daughter cards and on the backplane are identical. Since the AirMax VS[®] connector has a 1.3 mm offset between adjacent columns the same offset is assumed between adjacent rows in the footprint for all configurations. The footprints selected in this section are shown in figure 29.

Footprint (a) is a press-fit footprint. All other footprints are BGA or SMT footprints. Footprint (a) is the standard AirMax VS[®] press-fit footprint with a 1.3 mm offset. Footprint (b) is the AirMax VS[®] BGA footprint to be used if only routing between columns is required. Footprints (c) and (d) allow routing in both column and row direction. Footprint (c) is optimized for impedance. Footprint (d) is optimized for cross-talk. Footprint (e) allows double density routing. This means that the number of traces routed on a layer is doubled. The connector column pitch for all footprints is 2 mm. The drilled hole size for all press-fit footprints is 0.6 mm. The drilled hole size for all BGA or SMT footprints is 0.4 mm. The via pad size for the 0.6 mm drilled holes is 0.9 mm. For the 0.4 mm drilled hole a pad size of 0.7 mm is used. The anti-pad diameter for all via’s is 1.4 mm, except for footprint (e) where an anti-pad of 1.1 mm is used. The trace width for all footprints is 200 μm except for footprint (e) where a trace width of 140 μm is used. The trace width had to be reduced to allow double density routing with minimal cross-talk between the traces routed in the same column of the connector.



(a)



(b)

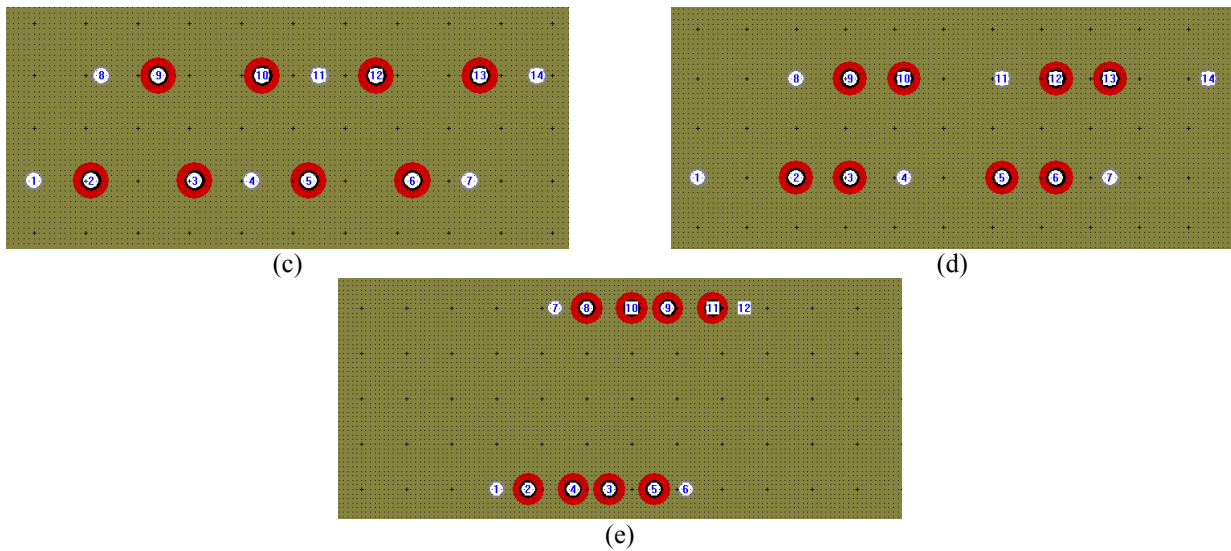


Figure 29: Footprints analyzed to determine impact of footprint on link level .

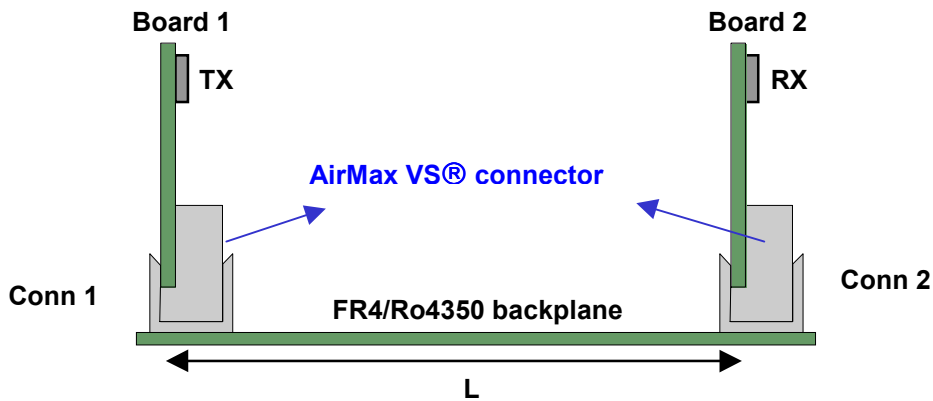


Figure 30: Backplane link

Figure 31 shows the signal integrity performance of the backplane links with FR4 material. Figure 31a and b show the insertion loss results. In figure 31a the backplane length is 5 cm, in figure 31b the length is 1 m. The link with the press-fit pins shows a ripple on the insertion loss. Apart from the double density routing structure, the insertion loss of all links with BGA footprint is comparable. Because of the smaller trace widths, the double density routing structure has higher losses.

Figure 31c shows the impedance of the 5 cm long link. Figure 31d shows the same results but zoomed in on the impedance of the footprint and first connector. The press-fit footprint causes a much higher impedance mismatch than the BGA footprints. The impedance-optimized footprint has the smallest impedance mismatch. The BGA footprint with 1.3 mm offset has a very good impedance match.

Figure 32 shows the cross-talk at receiver as a function of the backplane length for the different footprints. For long backplane lengths, the cross-talk in all links is comparable except for the footprint that allows double density routing. For short links the link with the cross-talk optimized footprint has the lowest cross-talk. It must be noted that although the footprint is optimized for cross-talk on a component level, on a link level this footprint will not necessarily result in the link with the lowest cross-talk. Cross-talk caused by the connectors combines with the cross-talk caused by the footprint, resulting in a lower or higher link cross-talk depending on the polarities of the via and connector cross-talk components.

Based on the results of figure 31 we can divide the links into 3 groups:

- Group 1: link with low impedance mismatch and low cross-talk: optimized BGA footprints (footprints b, c, and d)

Group 2: link with high impedance mismatch and low cross-talk: press-fit footprint (footprint a)

Group 3: link with low impedance mismatch and high cross-talk: double density routing footprint (footprint e)

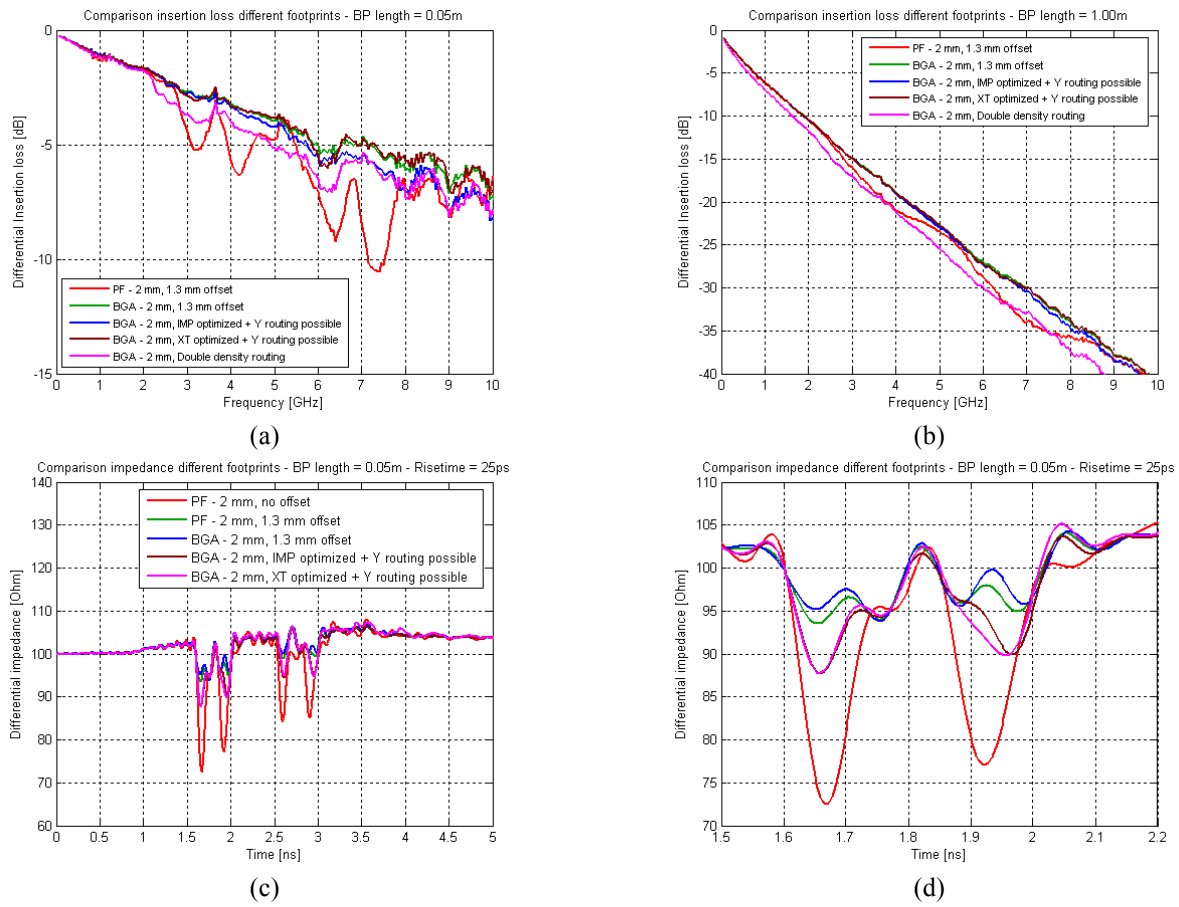


Figure 31: Insertion loss and impedance of considered backpanel links: (a) insertion loss 5 cm backpanel link, (b) insertion loss 1m backpanel link, (c) impedance 5 cm backpanel link, (d) impedance zoomed in on connector region.

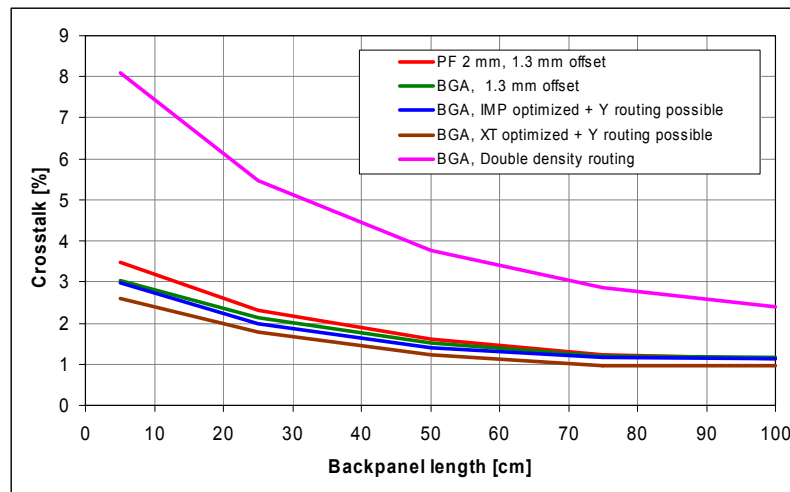


Figure 32: Cross-talk at receiver as function of backpanel length.

4.1 Performance measures

In this section we investigate the impact of the different footprint designs on link level performance. In section 4.2 the results when no signal conditioning is used are shown. In section 4.3 the results for a driver with 50 % de-emphasis are shown. As a performance measure, the eye height at the receiver

is used. In all simulations multi-line cross-talk is taken into account. Furthermore, it is assumed that a perfect driver without jitter or noise is used. Any jitter or noise at the receiver is coming from the interconnection link. For all simulations a PRBS (level 7) is used. Simulations have been performed for different lengths (5 cm, 25 cm, 50 cm, 1 m) and at different bitrates (from 1 Gb/s up to 10 Gb/s) in order to determine at which frequency and which lengths BGA footprints offer a performance advantage over press-fit footprints. It is assumed that the risetime and fall time of the signals is identical to 1/3 of the bit time.

4.2 Without signal conditioning

Figure 33 shows the eye height as a function of the bitrate for the different considered footprints and for the different lengths. It is clear that for short lengths and above 3 Gb/s the links belonging to group 1 perform better than the links belonging to groups 2 and 3. The same conclusion can be drawn for the links with the 25 cm long backplane. If we increase the backplane length further, we notice that the performance difference between the different groups becomes smaller: link performance is dominated by backplane losses and not by impedance matching of the footprint. Also notice that as the length increases, the impact of trace widths becomes more important. For all footprints 200 μm width traces were used, except for the footprint that allows double density routing. For this footprint the trace width is 140 μm .

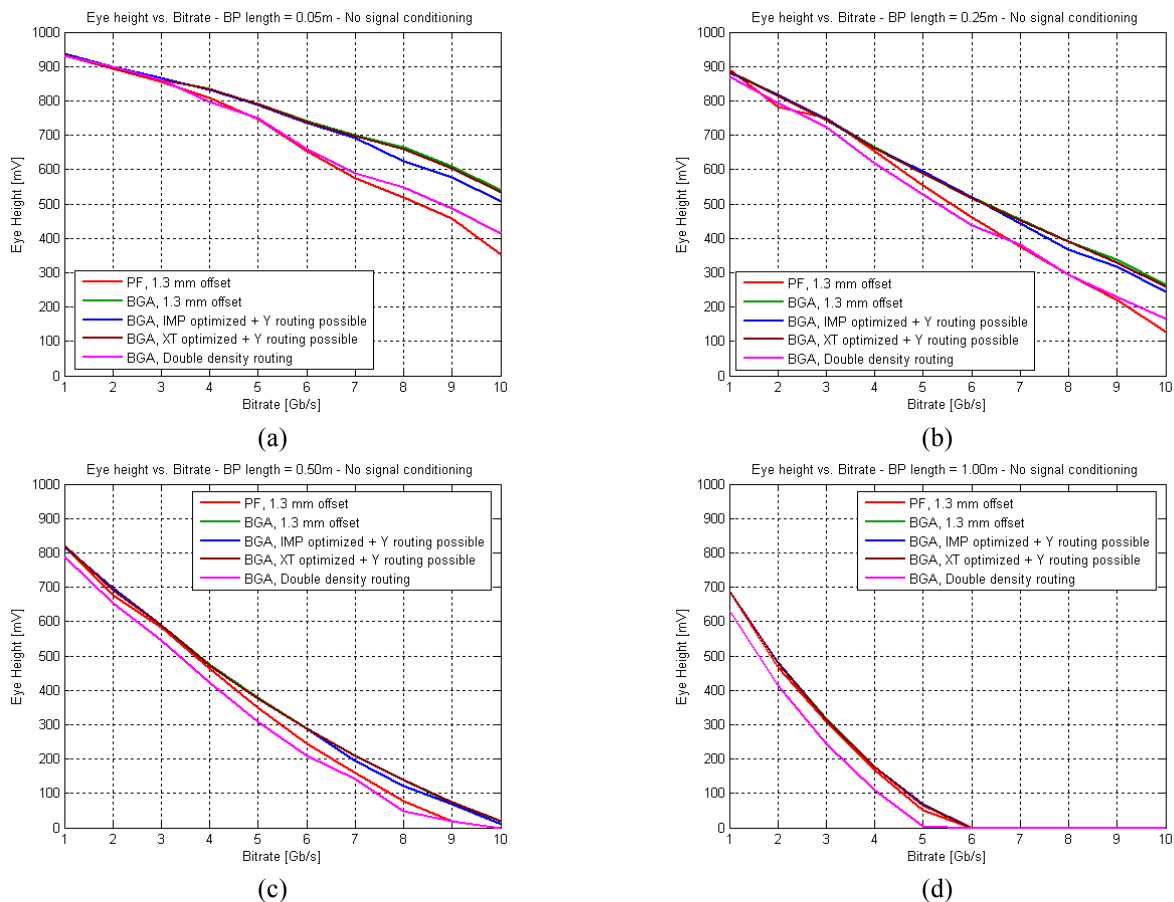


Figure 33: Eye height as function of bitrate for the different footprints, no signal conditioning used, FR4: backpanel length 5 cm (a), backpanel length 25 cm (b), backpanel length 50 cm (c), backpanel length 1 m (d).

To reduce the impact of the trace losses similar simulations were also performed with Ro4350 material instead of FR4 (for both the backpanel and the daughter cards). A dielectric constant of 3.5 and a loss tangent of 0.005 were assumed in this case. The results are shown in figure 34. The performance difference between the press-fit and the BGA footprints is more apparent, also for longer lengths. In case of a 1 m backpanel the performance of the press-fit and the BGA footprints is similar up to 4 to 5 Gb/s. From about 5 Gb/s on there is a clear benefit in using a BGA footprint.

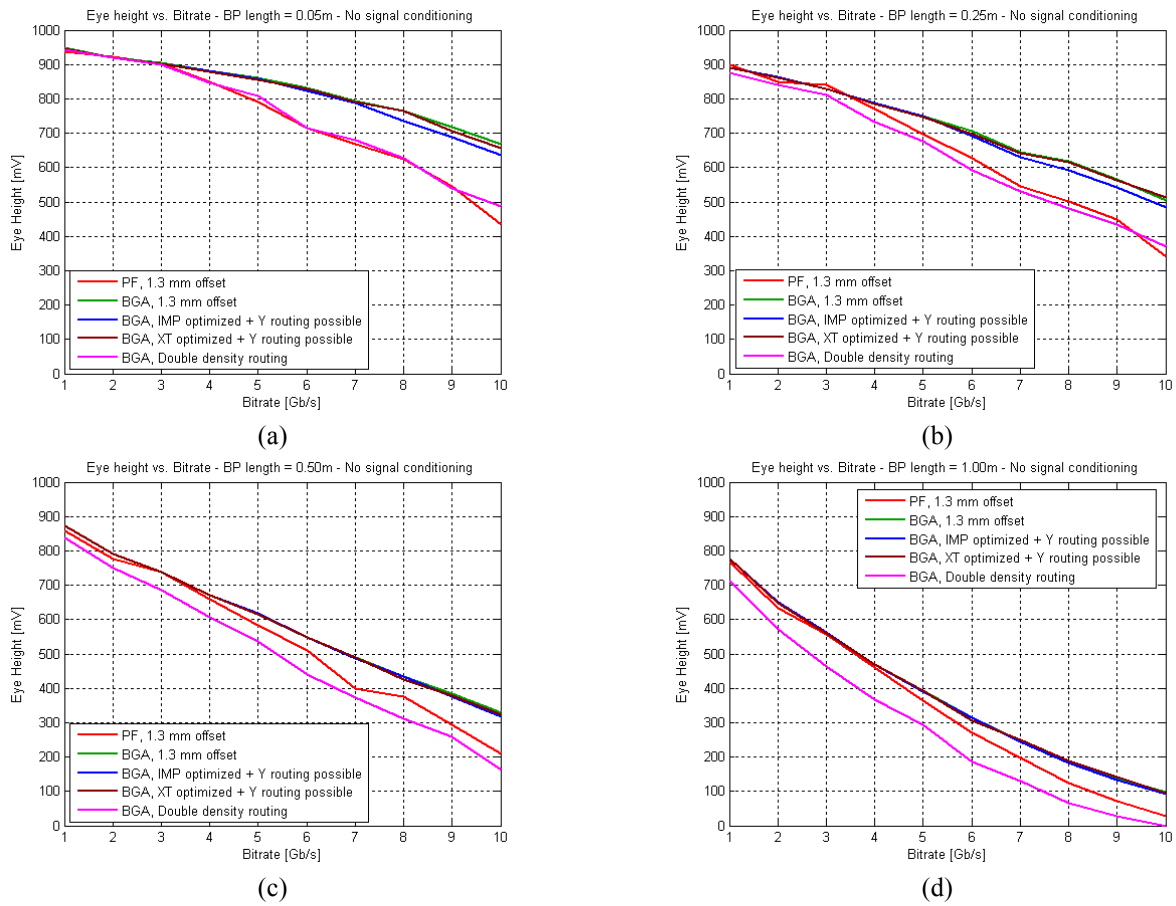
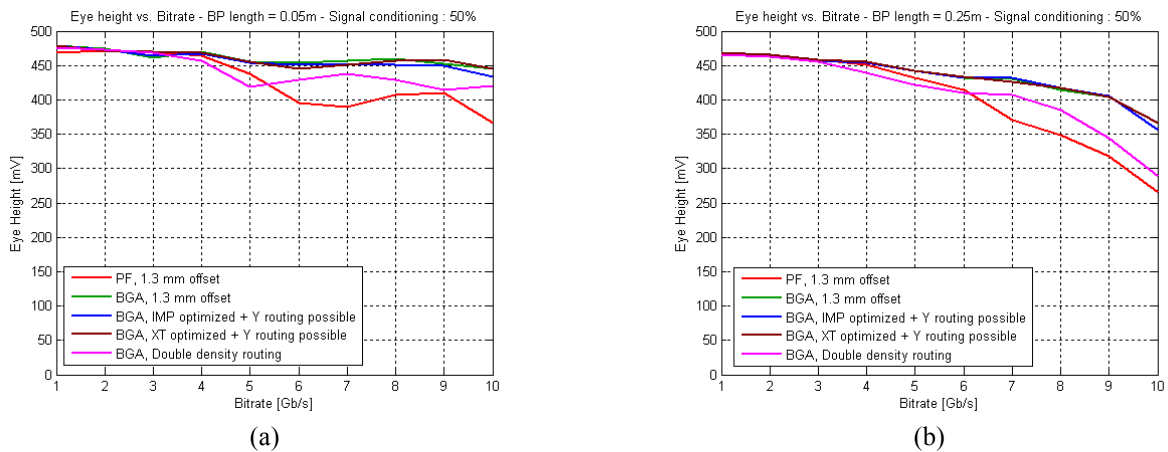


Figure 34: Eye height as function of bitrate for the different footprints, no signal conditioning used, Ro4350: backpanel length 5 cm (a), backpanel length 25 cm (b), backpanel length 50 cm (c), backpanel length 1 m (d).

4.3 With signal conditioning

Figure 35 shows the same results as figure 33, except this time a source with 50 % de-emphasis is used. Figure 36 shows the results when Ro4350 material is used for the backpanel and the daughter cards. The same conclusions can be drawn from these results as in the previous section.



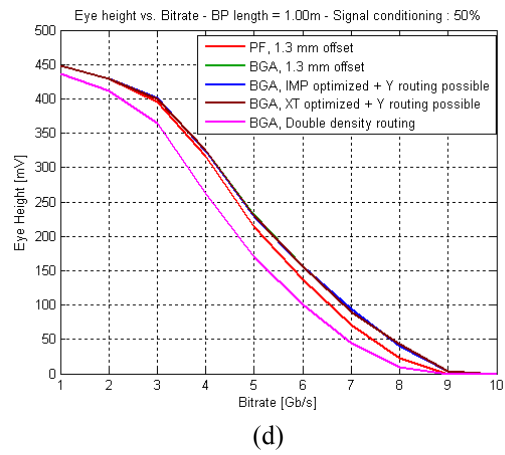
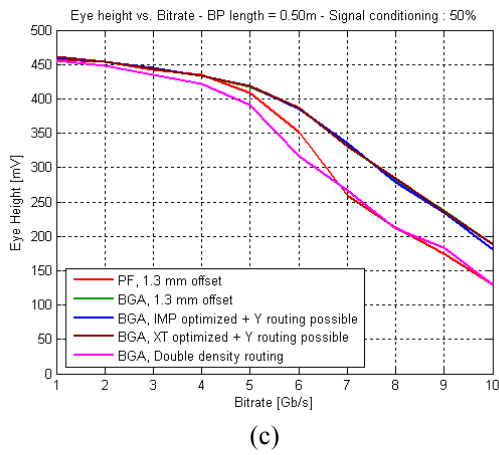


Figure 35: Eye height as function of bitrate for the different footprints, driver with 50 % de-emphasis, FR4: backpanel length 5 cm (a), backpanel length 25 cm (b), backpanel length 50 cm (c), backpanel length 1 m (d).

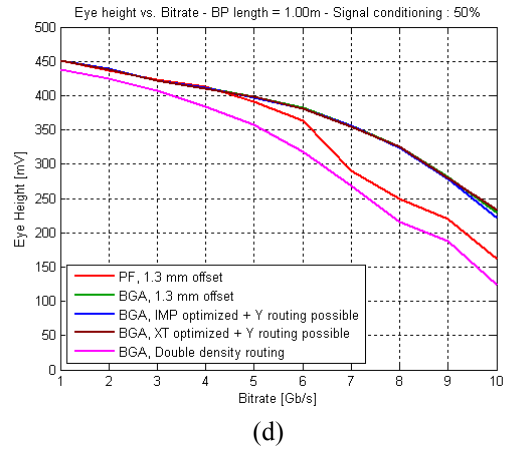
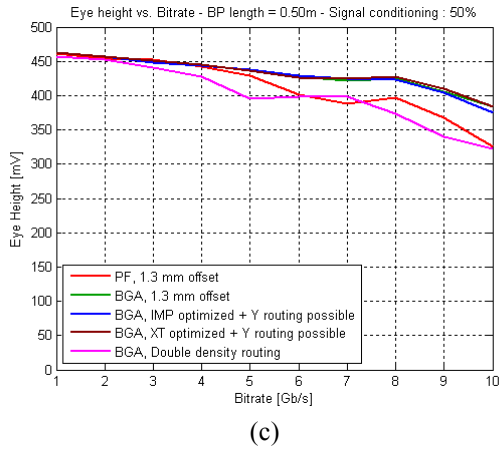
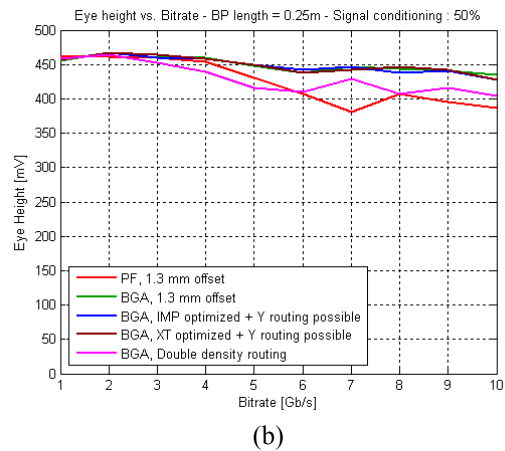
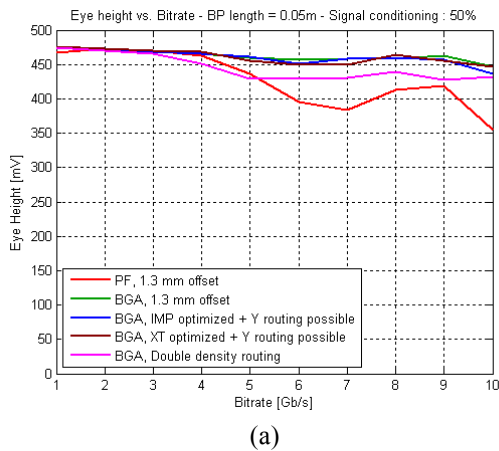


Figure 36: Eye height as function of bitrate for the different footprints, driver with 50 % de-emphasis, Ro4350: backpanel length 5 cm (a), backpanel length 25 cm (b), backpanel length 50 cm (c), backpanel length 1 m (d).

5 Conclusions

In this paper the performance of connector footprints is studied. The footprint of press-fit connectors is highly determined by the connector itself: the drilled hole size and the position of the signal and ground via holes is fixed. Remaining via hole parameters such as via pad size and anti-pad size give only limited performance benefit. Increasing the anti-pad diameter results in improved insertion loss and impedance but once the anti-pad has a certain size, only a non-significant improvement can be made by further increasing the anti-pad size. Furthermore, increasing the anti-pad decreases the space available for routing traces in the connector footprint region significantly. If connector footprint optimization is required and a press-fit connector needs to be used, then a connector with

optimized footprint needs to be used. This means a connector with staggered signal pairs and with a sufficient large column-to-column pitch. If the correct pair-to-pair offset is used then staggered pairs can reduce the cross-talk in the connector significantly. Furthermore the column pitch needs to have the correct size to allow routing of traces with the required trace width and with a sufficiently large anti-pad: routing traces with a width of 200 μm requires a column pitch of 2 mm. If two pairs need to be routed in the column direction (double density routing) then a minimal column-to-column pitch of 3 mm is required. Double density routing is very interesting since it allows reducing the number of signal layers, making the PCB more cost-effective.

BGA connectors have the advantage that the position and size of the via holes can be separated from the connector footprint design. This means that if the connector does not have an optimized footprint, by changing the relative position of the via holes the footprint can be optimized for impedance, cross-talk and/or routing density. Significant performance improvement can also be obtained if via holes with a smaller drill size are used.

Looking on an application level, BGA footprints have advantages for both low speed and high-speed applications. The routing flexibility associated with BGA connectors makes sure double density routing is possible, even for connectors on a 2 mm column pitch. Above 3 GHz the optimized footprint performance makes sure that BGA connectors have a significant performance improvement over press-fit connectors, especially for applications with short lengths. For applications with longer lengths the performance improvement resulting from using BGA footprints is most apparent for low loss materials. In case of FR4 the link performance is dominated by backplane losses and not by impedance matching of the footprint.

6 References

- [1] E. Laermans, J. De Geest, D. De Zutter, F. Olyslager, S. Sercu and D. Morlion, "Modeling Differential Via Holes", Proc. of the 9th Topical Meeting on Electrical Performance of Electronic Packaging, Scottsdale, Arizona, Oct. 2000, pp. 127-130.
- [2] E. Laermans, J. De Geest, D. De Zutter, F. Olyslager, S. Sercu and D. Morlion, "Modeling Differential Via Holes", IEEE Trans. on Advanced Packaging, Vol. 24, No 3, Aug. 2001, pp. 357-363.
- [3] E. Laermans, J. De Geest, D. De Zutter, F. Olyslager, S. Sercu and D. Morlion, "Modeling Complex Via Hole Structures", Proc. of the 10th Topical Meeting on Electrical Performance of Electronic Packaging, Cambridge, Massachusetts, pp. 149-152, Oct. 2001.
- [4] E. Laermans, J. De Geest, D. De Zutter, F. Olyslager, S. Sercu and D. Morlion, "Modeling Complex Via Hole Structures", Accepted for publication in IEEE Trans. on Advanced Packaging, Aug. 2002.