

**Customer Measurement Report:**  
**BergStak<sup>®</sup> 0.8 mm Mezzanine Connectors**  
**SMT Vertical Header to SMT Vertical Receptacle**  
**12 mm Board-to-Board Stack Height**  
**Part Numbers: 61083, 61082**

**vs. PCIe<sup>®</sup> Gen 2, 3**

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## ***Purpose:***

- To verify whether the measured performance of BergStak® 12 mm stack height connector meets the PCI Express Gen2 electrical requirements
  - PCIe Gen2 Specification
    - 85 ohms reference impedance
    - Data rate: 5 GT/s
  - Additional data such as impedance and power-summed crosstalk, which are not part of the PCIe Gen2 specification, are also shown

## ***Conclusion:***

- BergStak® 12 mm stack height connector **MEETS THE PCI EXPRESS GEN2 SPECIFICATION**
- Lower stack-heights should perform similarly or better

- The specific performance and compliance requirements proposed by the PCIe<sup>®</sup> Gen 3 CEM working group have been reviewed by FCI.
- Information shown in this report for PCIe<sup>®</sup> Gen 2 is compatible with PCIe<sup>®</sup> Gen 3.
- FCI will provide compliance details when PCIe<sup>®</sup> Gen 3 is released to the public

## Test Samples

- BergStak<sup>®</sup> vertical plug, P/N 61083-064402LF, was tested mated to BergStak<sup>®</sup> vertical receptacle, P/N 61082-062402LF (shown in Fig. 1)

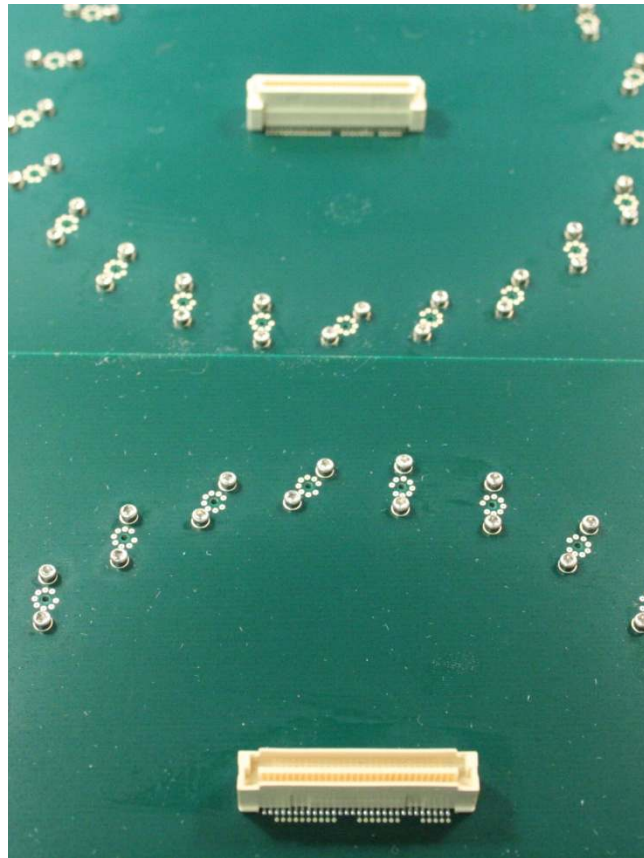
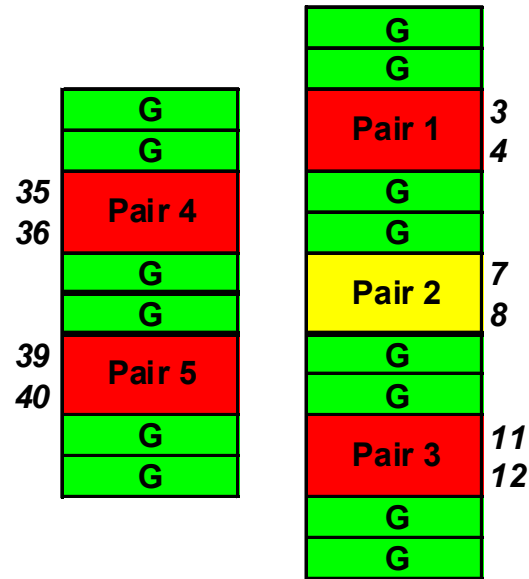


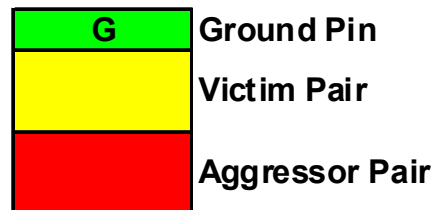
Figure 1 – BergStak 12 mm Stack Height Connectors on test boards

# Wiring Pattern Measured



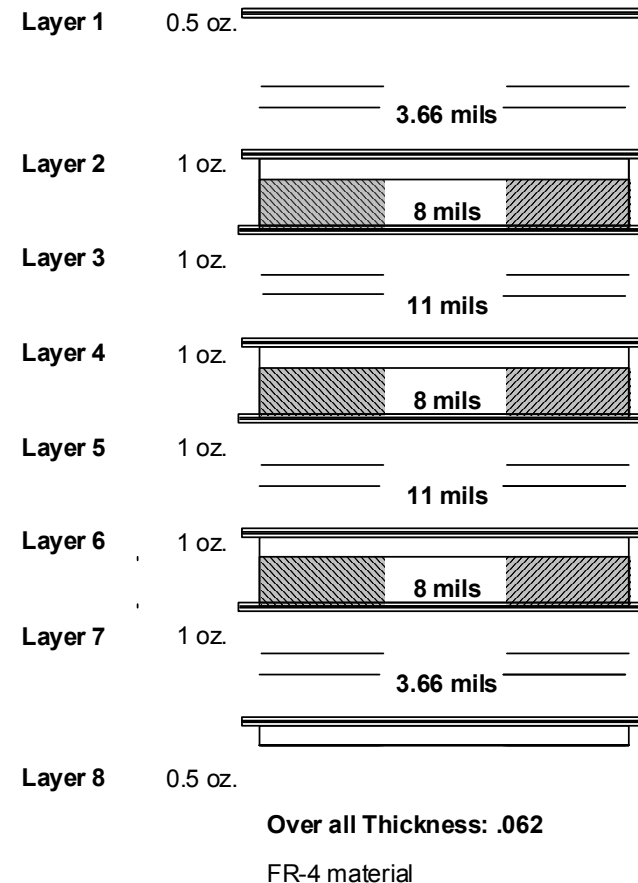
GGSSGG

Key:



- All test boards are eight-layer, 0.062 mil thick, made with FR-4 board material ( $\epsilon_r=4.3$ ,  $df = 0.019$ ). Trace length from SMA to via is 1.78 inches, and calibration traces are 3.56 inches.
- All traces are routed on layer 6.

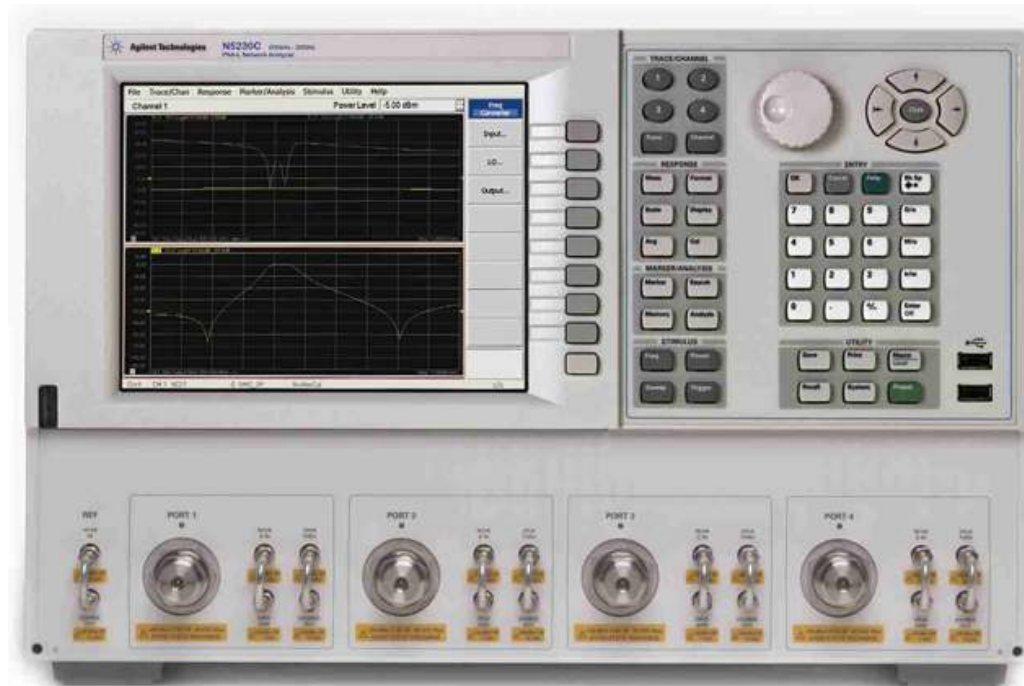
## DIELECTRIC STACK-UP



## Frequency-domain Data

- The data was renormalized to a reference impedance of 42.5 ohms for the purposes of creating this report
- Return Loss and Insertion Loss were plotted from the plug to the receptacle side.
- Insertion Loss of the 2x calibration trace was subtracted from the insertion loss of each pair.
- Near-end Crosstalk was measured and plotted on the plug side.
- All time-domain data was taken in the Frequency-domain and transformed into the Time-domain in MATLAB.
- Test fixtures were removed using Agilent's automatic fixture removal function

- Agilent Technologies N5230CA PNA-L Network Analyzer
  - Frequency Range: 300 KHz – 20 GHz
- Calibration Used:
  - SOLT calibration from 10 MHz to 20 GHz with 2000 data points and having an IF Bandwidth of 1 KHz



Stock Photo taken from [www.home.agilent.com](http://www.home.agilent.com)

# PCI Express Gen2 Requirements



Table 5-3: Signal Integrity Requirements and Test Procedures for 5 GT/s Support

Parameter	Procedure	Requirements
Differential Insertion Loss (DDIL)	EIA 364-101 The EIA standard shall be used with the following considerations: 1. The measured differential S parameter shall be referenced to an 85 Ω differential impedance. 2. The test fixture shall meet the test fixture requirement defined in Section 5.4.2. 3. The test fixture effect shall be removed from the measured S parameters. Refer to Note 1.	≥-0.5 dB up to 2.5 GHz; ≥-[0.8*(f-2.5)+0.5] dB for 2.5 GHz < f ≤ 5 GHz (for example, ≥-2.5 dB at f = 5 GHz); ≥-[3.0*(f-5)+2.5] dB for 5 GHz < f ≤ 7.5 GHz (for example, ≥-10 dB at f = 7.5 GHz)
Differential Return Loss (DDRL)	EIA 364-108 The EIA standard shall be used with the following considerations: 1. The measured differential S parameter shall be referenced to an 85 Ω differential impedance. 2. The test fixture shall meet the test fixture requirement in Section 5.4.2. 3. The test fixture effect shall be removed. Refer to Note 1.	≤ -15 dB up to 3.0 GHz; ≤ -5 dB for 3.0 GHz < f ≤ 5 GHz; ≤ -1 dB for 5.0 GHz < f ≤ 7.5 GHz
Intra-pair Skew	Intra-pair skew must be achieved by design; measurement not required.	5 ps max
Differential Near End Crosstalk (DDNEXT)	EIA 364-90 The EIA standard must be used with the following considerations: 1. The crosstalk requirement is with respect to all the adjacent differential pairs including the crosstalk from opposite sides of the connector, as illustrated in Figure 5-4. 2. This is a differential crosstalk requirement between a victim differential signal pair and all of its adjacent differential signal pairs. The measured differential S parameter shall be referenced to an 85 Ω differential impedance.	≤ -32 dB up to 2.5 GHz; ≤ -26 dB for 2.5 GHz < f ≤ 5.0 GHz; ≤ -20 dB for 5.0 GHz < f ≤ 7.5 GHz

Notes:

1. The specified S parameters requirements are for connector only, not including the test fixture effect. While the TRL calibration method is recommended, other calibration methods are allowed.

PCIe Gen2 (5.0 GT/s) specifies the following electrical requirements

- Differential Insertion Loss
- Differential Return Loss
- Intra-pair Skew
- Differential multi-active NEXT

NOTE:

- **Reference impedance** for these requirements is **85 ohms**
- Specification applies only to the connector interface (which includes the **connector and the edge finger pads**). Other fixture effects must be removed.

- Historically, the power-sum method has been used to calculate the sum of crosstalks from multiple aggressors

$$\text{Power Sum } XT = 10 \log_{10} \left( \sum_n |XT_n|^2 \right)$$

- In PCIe specifications, an alternative method has been used to calculate the crosstalk sum (referred to as “DDNEXT” or “Multi-active Crosstalk” in this report)

$$XT \text{ Sum } PCIe = 20 \log_{10} \left( \sum_n XT_n \right)$$

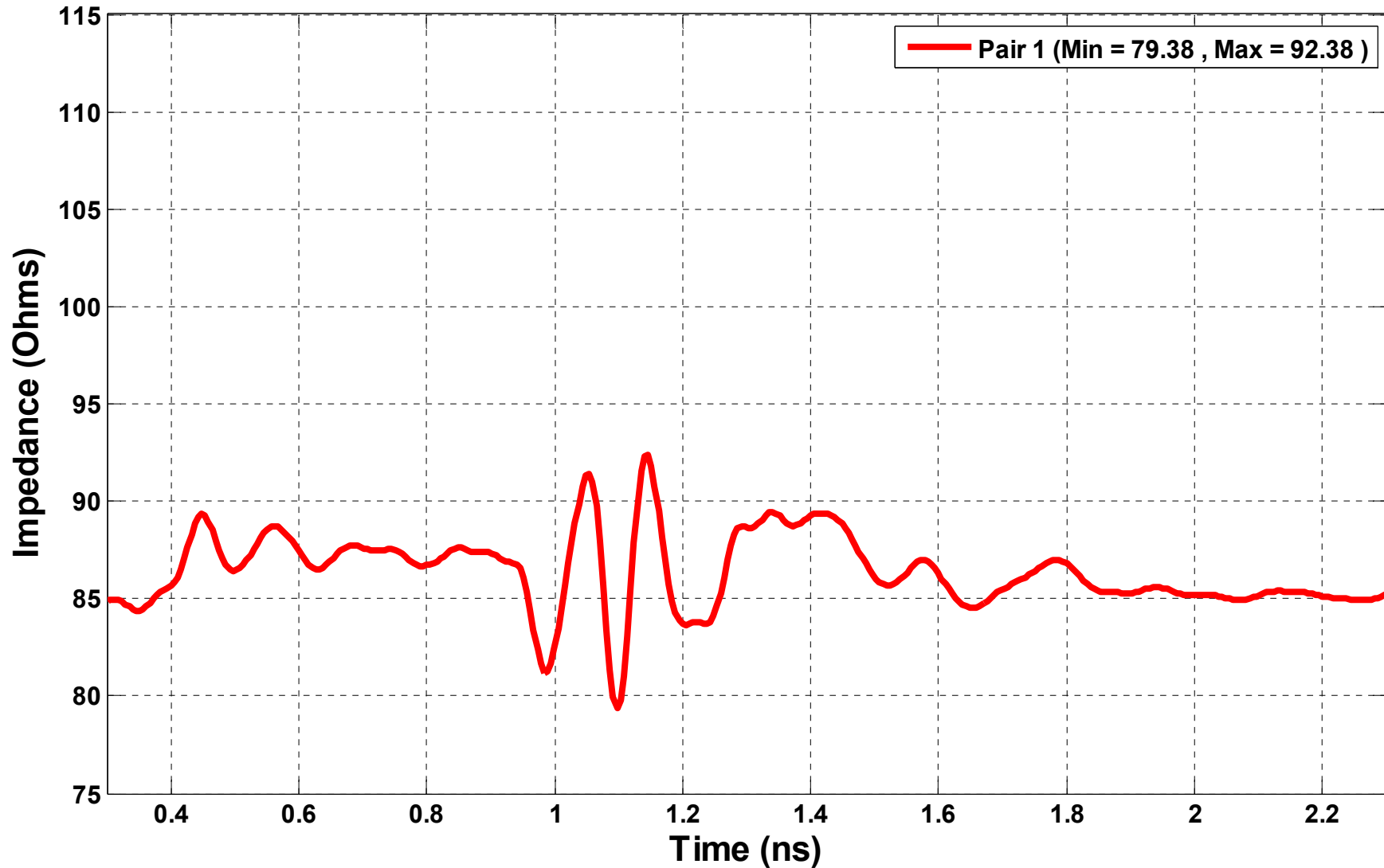
Where  $XT_n$  is the differential crosstalk S-parameter from aggressor #n

- Both power-sum and multi-active crosstalk plots are shown in this report

# Differential Impedance



## FCI 12mm GGSSGG Compared to PCIe Gen2 Rev 2.0 - Differential Impedance Risetime = 30 ps (20-80%)

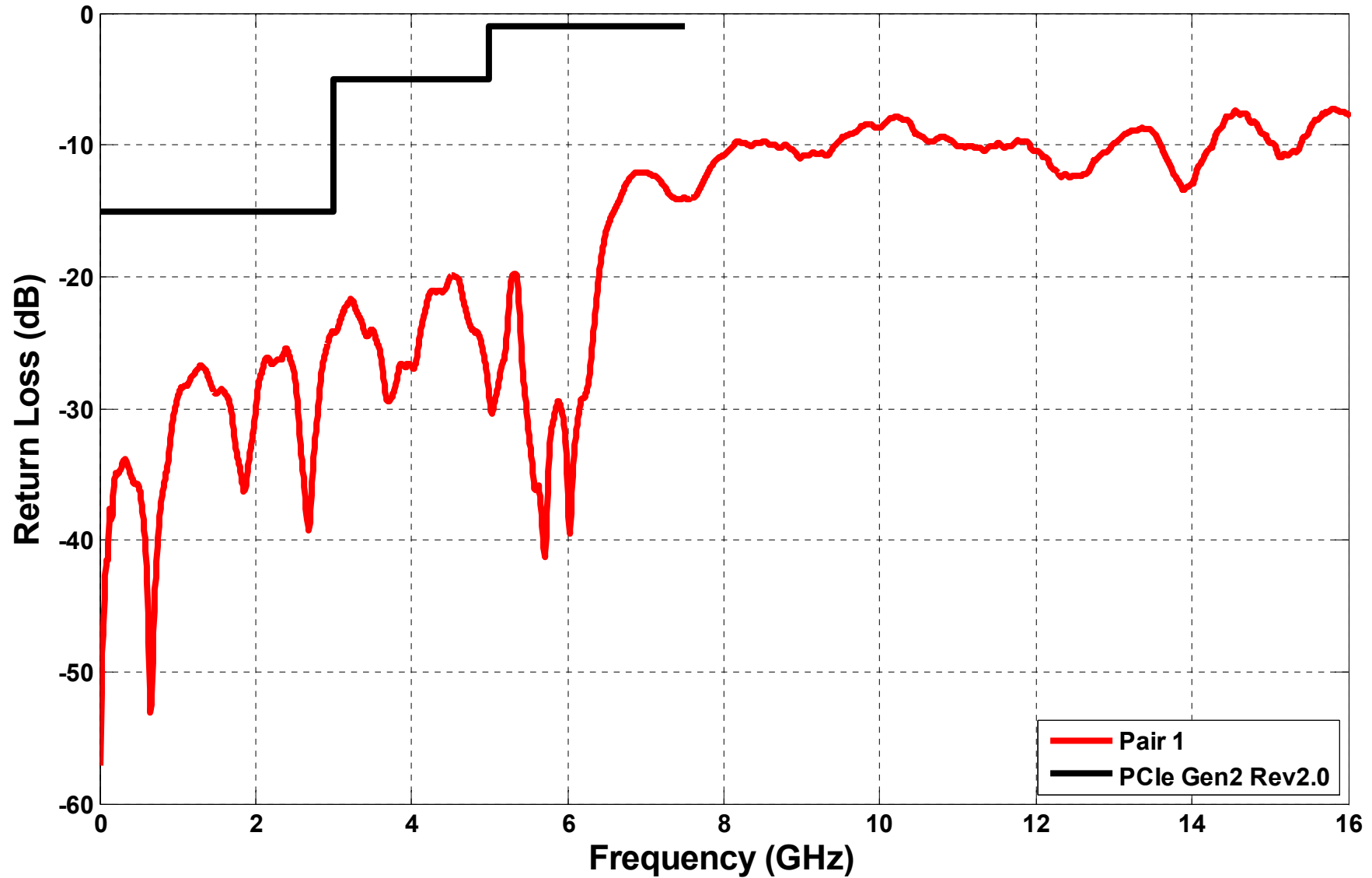


Impedance is not a requirement in the spec. It is provided as additional information.

# Differential Return Loss



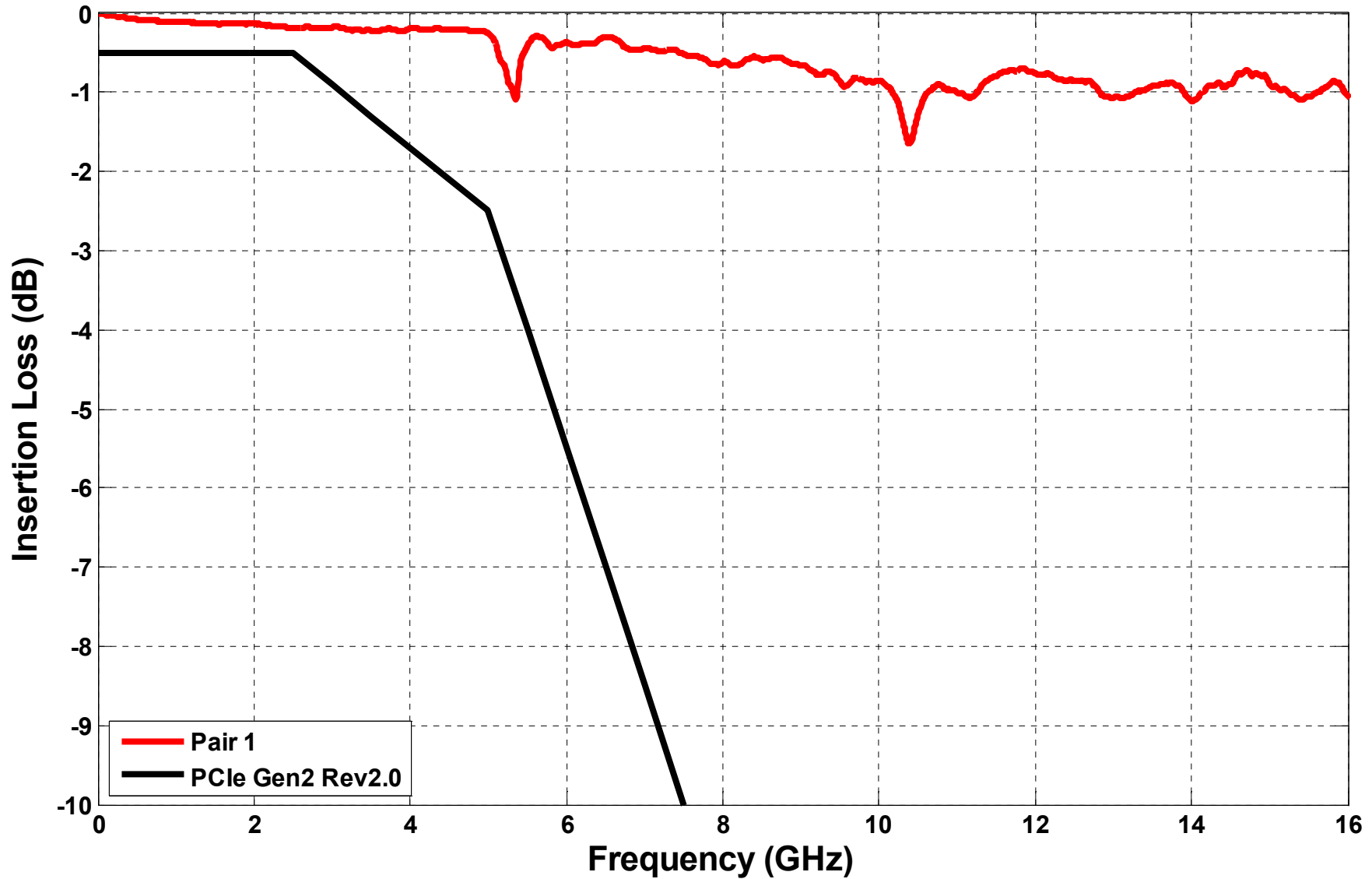
## FCI 12mm GGSSGG Compared to PCIe Gen2 Rev 2.0 - Differential Return Loss



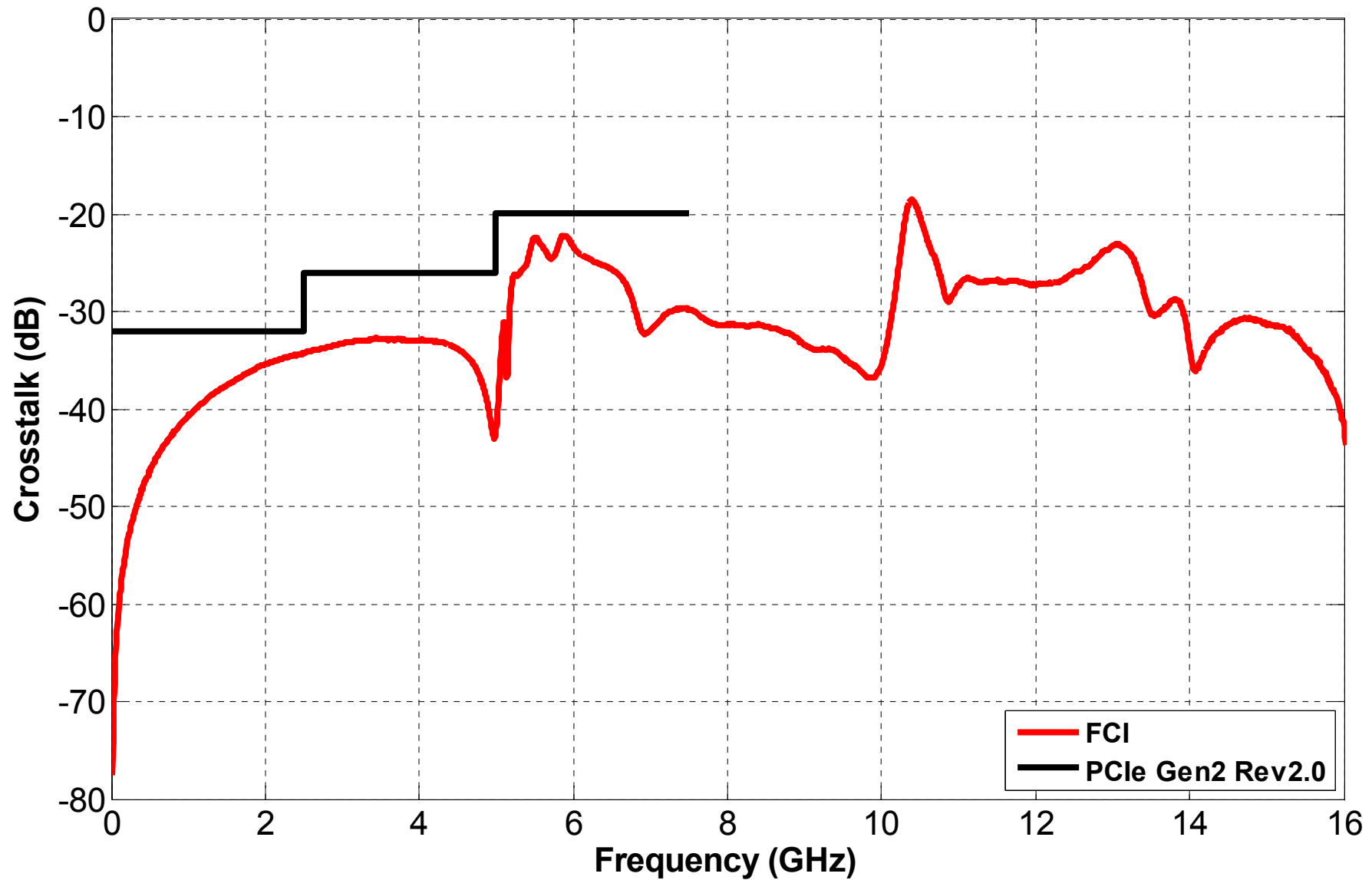
# Differential Insertion Loss



## FCI 12mm GGSSGG Compared to PCIe Gen2 Rev 2.0 - Differential Insertion Loss



## Pair 2 - Multi-active NEXT

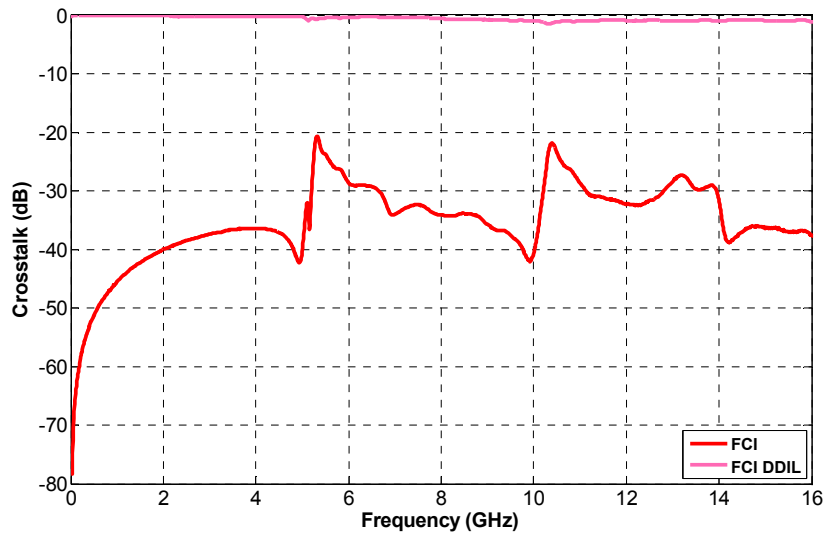


# Power-Summed Crosstalk



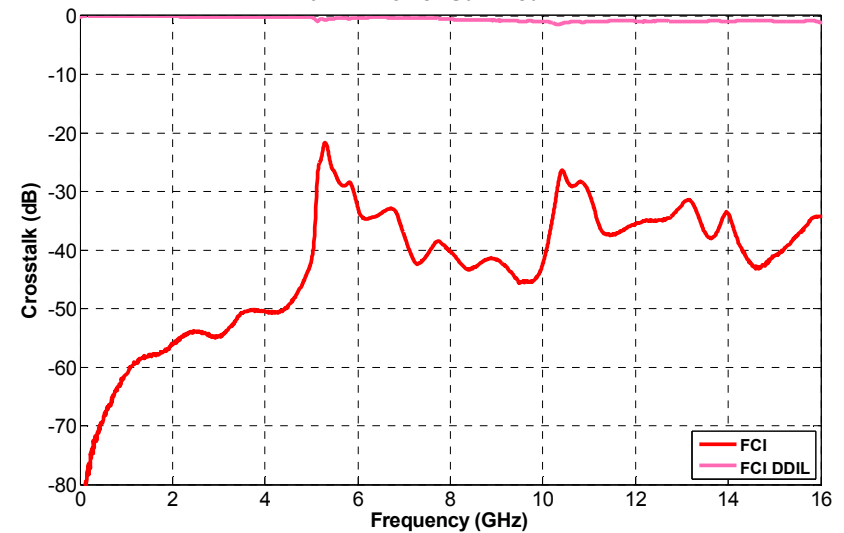
## Near-end Crosstalk

Pair 2 - Power-Summed NEXT



## Far-end Crosstalk

Pair 2 - Power-Summed FEXT



Power-summed Crosstalk is not a requirement in the spec. It is provided as additional information.