Improving System Performance by Reducing System Impedance to 85 Ohms

DesignCon 2007 – TA4-2

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Agenda

- Examine a high-speed differential link that might be found in a future server.
- Evaluate features that might need optimization if transfer rates are ever to approach 10 GT/S.
- Propose a solution.
- Simulated/measured data.

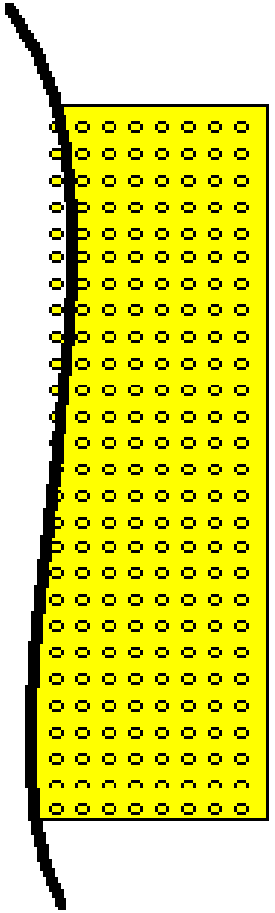
Ground Rules

- It is presumed the board material of choice is FR4.
- It is presumed that server signal links will require one, sometimes two, in-line connectors.
- It is presumed that baseboards will have to be at least 0.09 inches thick, sometimes thicker.
- It is presumed that transmit power is limited.

The Interconnect Circuit

- Packages
  - Optimizations?
- Vias
  - Optimizations?
- FR4
  - Account for tolerances
- Connectors
  - Choices

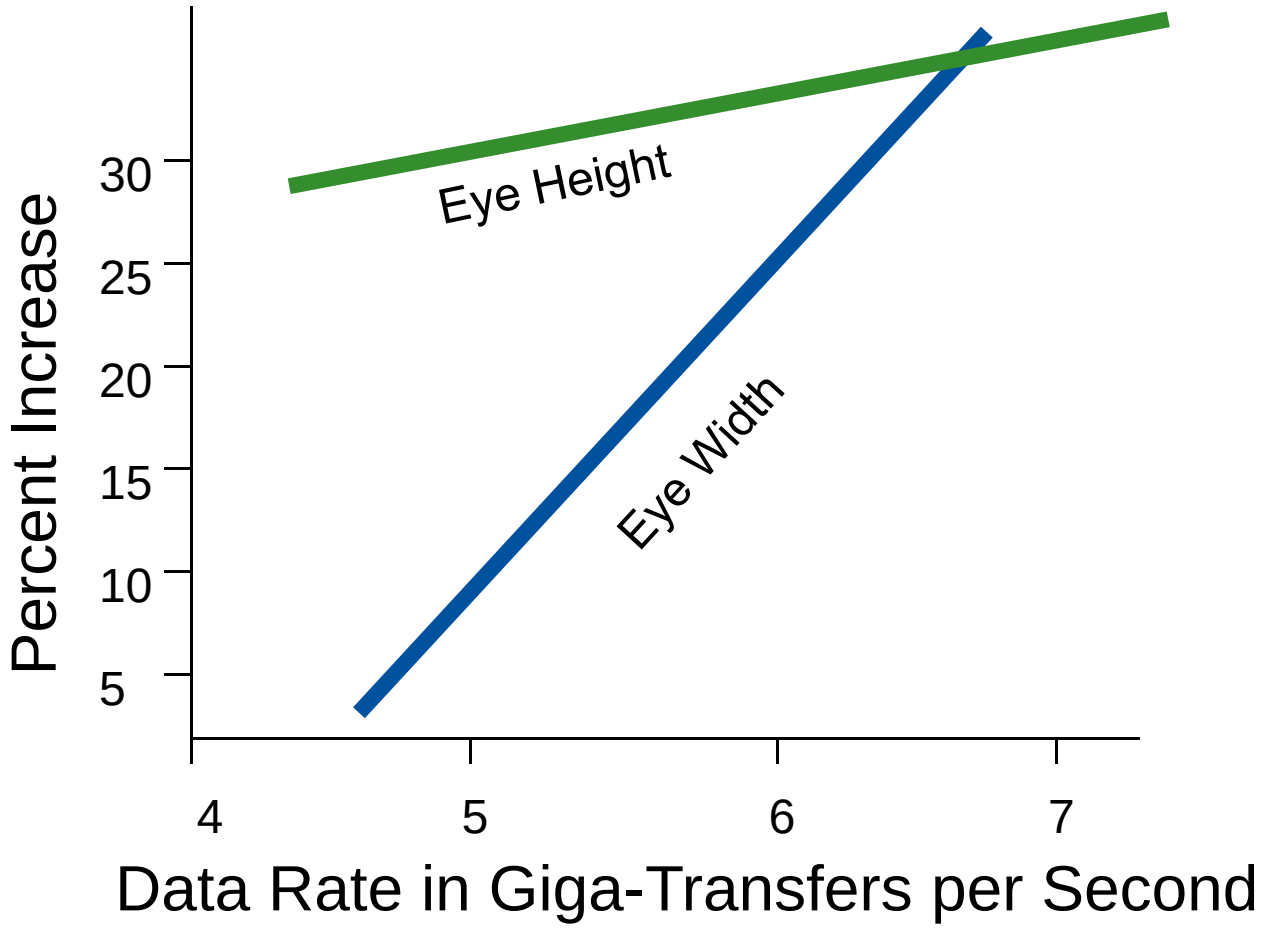
The Package



In a high pin-count package, routing channels get used up very quickly – forcing a choice: more layers, or finer lines?

It is true under the package. It is true inside the package.

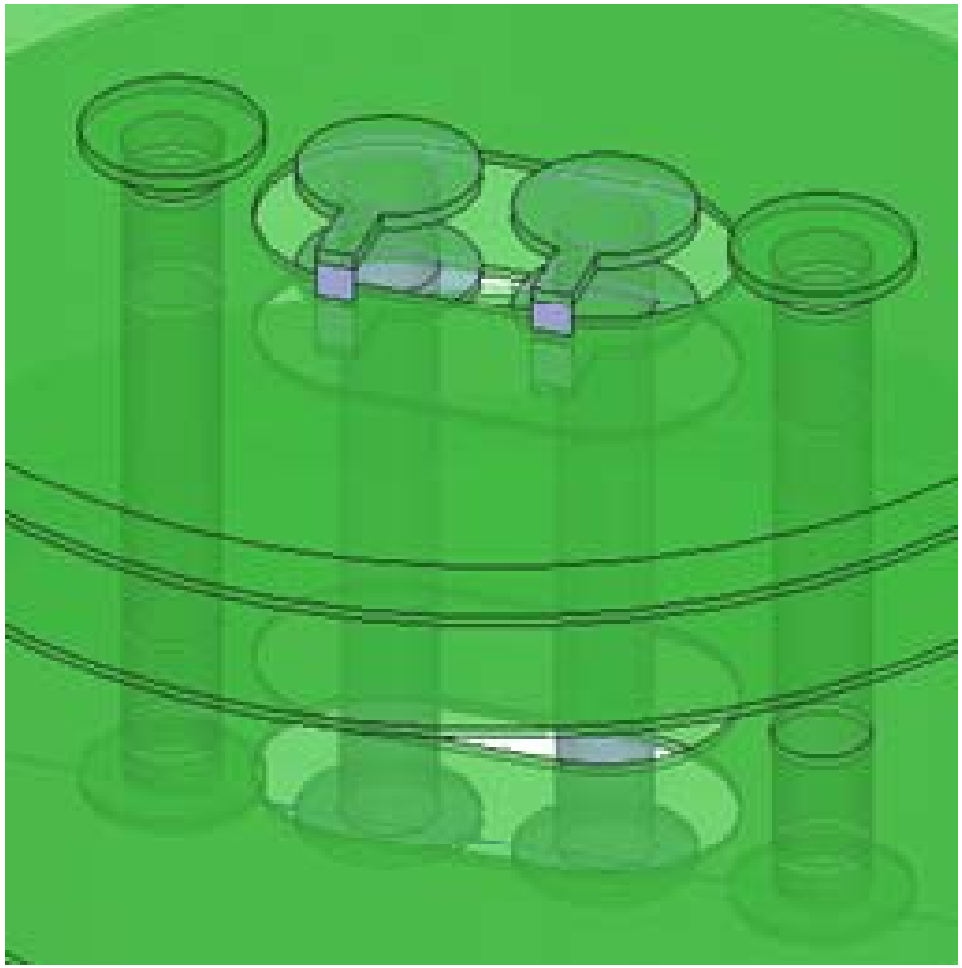
Projected Benefits of 85ohm Packages for High-Speed Links



Vias

- There will have to be vias under each package at the ends of the link.
- There will have to be vias at most connectors.
- It is presumed that through-hole vias will be used wherever possible.

Simulated Through-Hole Vias

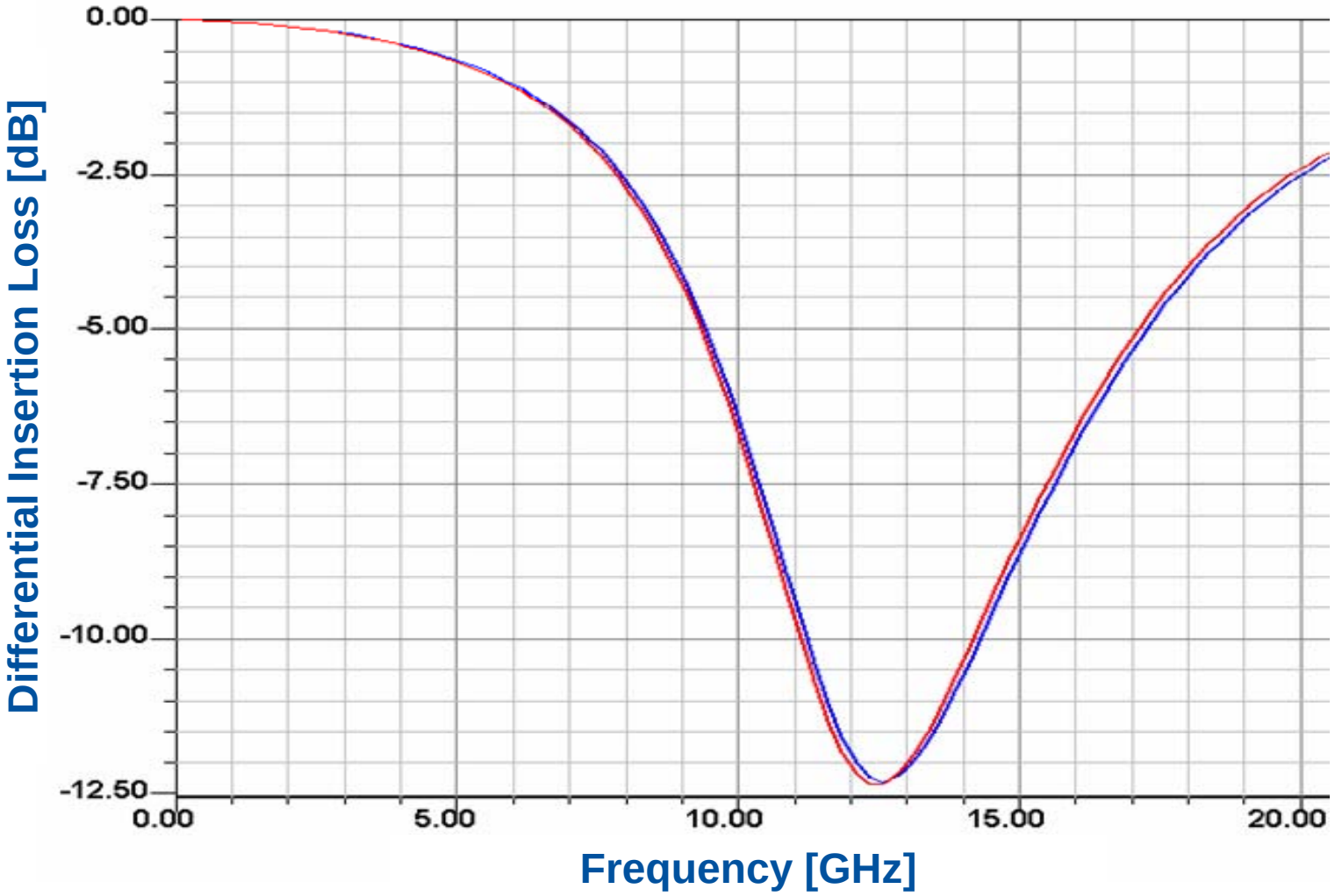


Signals are routed differentially. Therefore vias are paired and benefit from nearby ground vias.

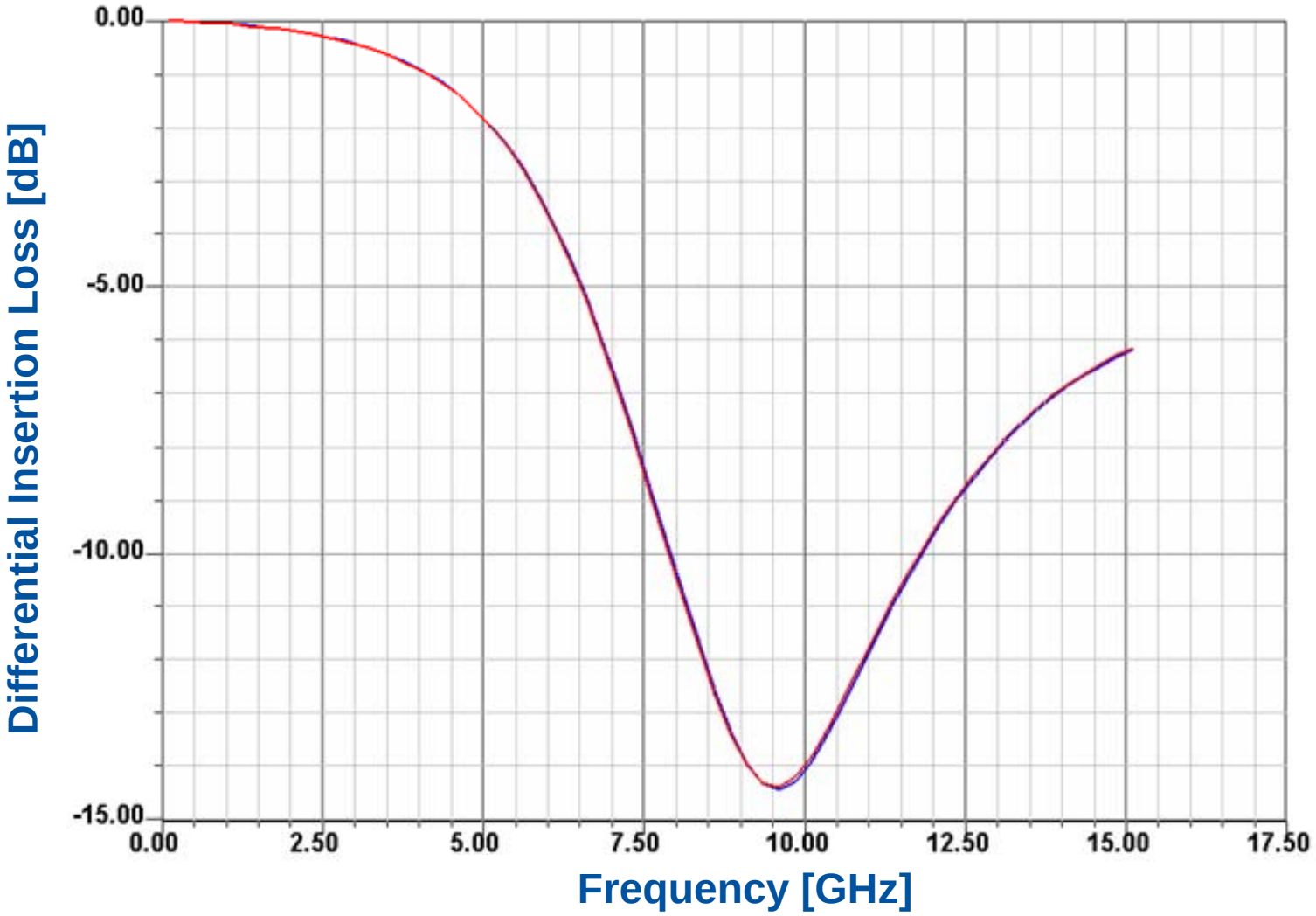
Issues with Vias

- Count the top microstrip layer as layer 1.
- Below it is a reference plane, layer 2.
- Below that is a stripline layer, layer 3.
- By this count, the worst case through-hole via is always the via that routes signal from layer 1 to layer 3.
- The problem is the resonant stub below layer 3

Frequency Response of a 10mil Through-Hole Via



Frequency Response of a 24mil Through-Hole Via



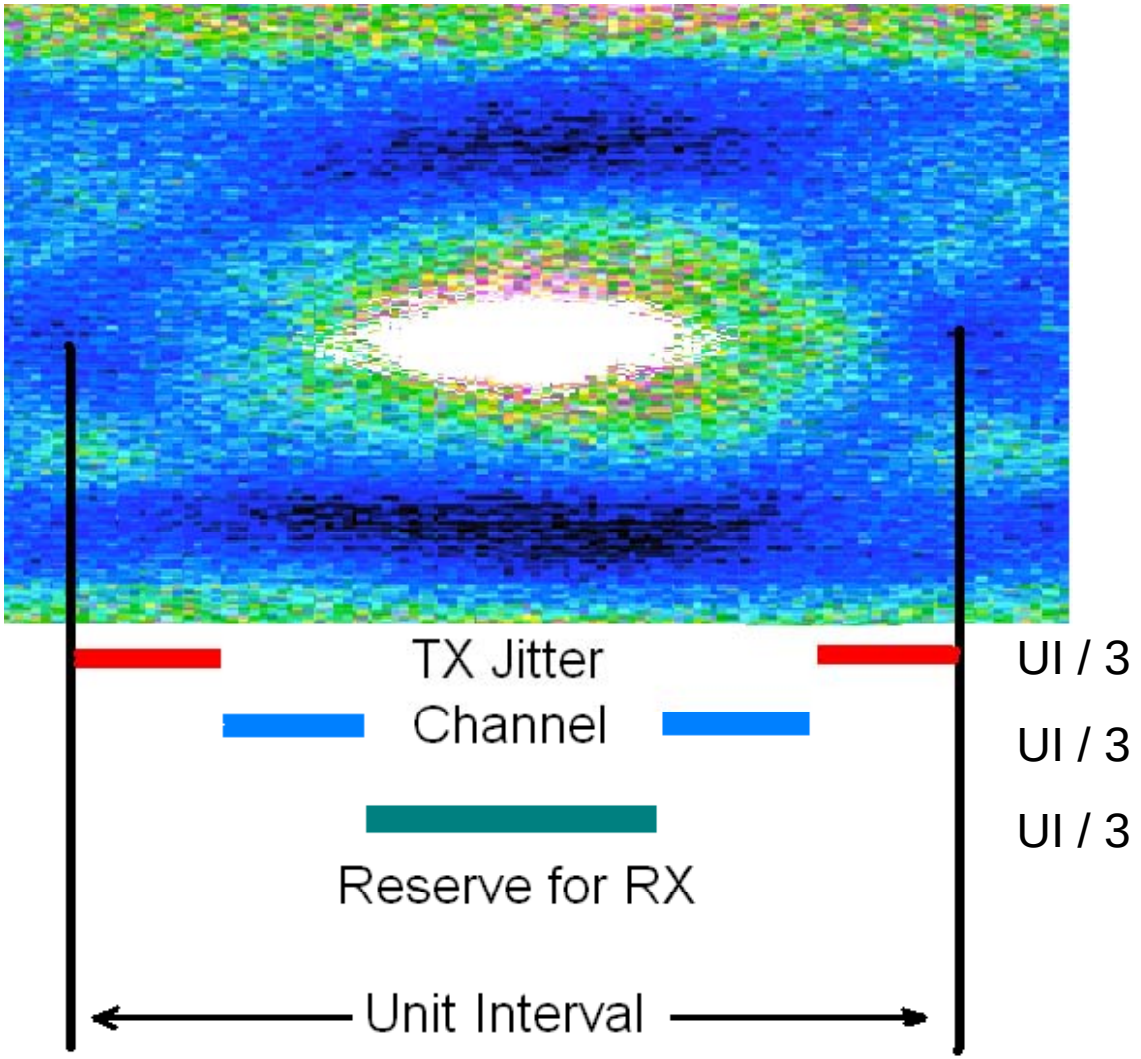
FR4

- Yes, FR4 is lossy but that can be easily compensated.
- The real problem is impedance tolerances.
- Impedance mismatches produce reflections and sometimes resonances.
  - Package to board
  - Board to connector
  - Board to board
- Reflections cause timing jitter.

The Budget

- Total eye width at 10GT is 100ps.
- Typically the timing budget is approximately:
  - 1/3 Unit interval jitter out of the transmitter
  - 1/3 Unit interval jitter available for the interconnect circuitry
  - 1/3 Unit interval eye opening required at the receiver input.
- Total jitter produced by package to board interfaces, vias, connectors, board to board impedance mismatches, and crosstalk, should be less than about 30ps.

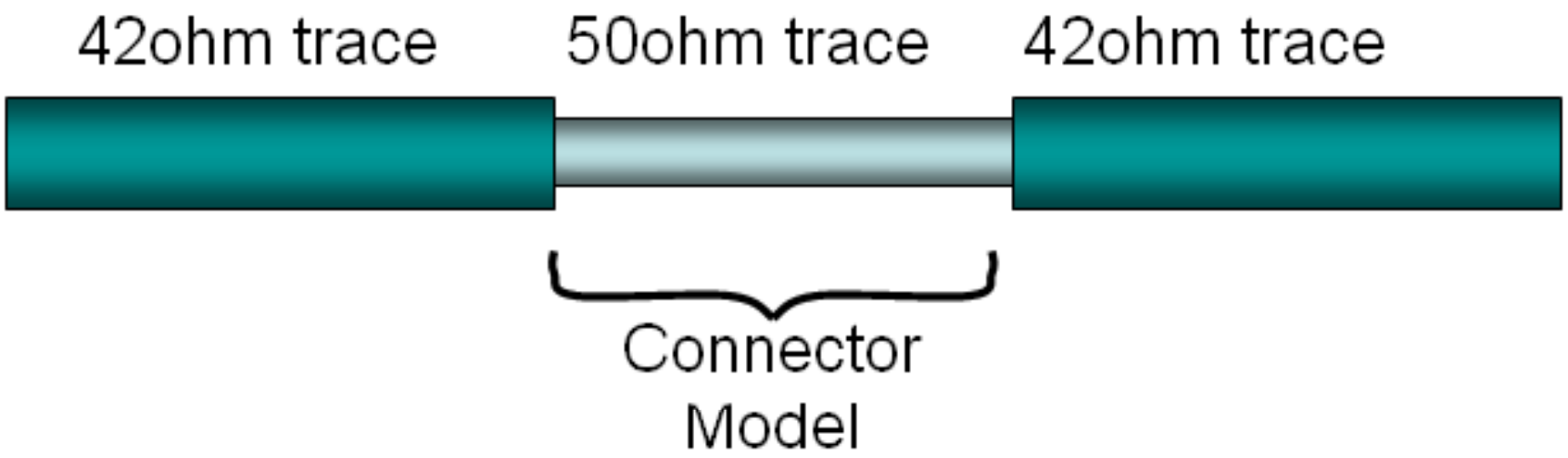
Eye Opening Budget Allocation



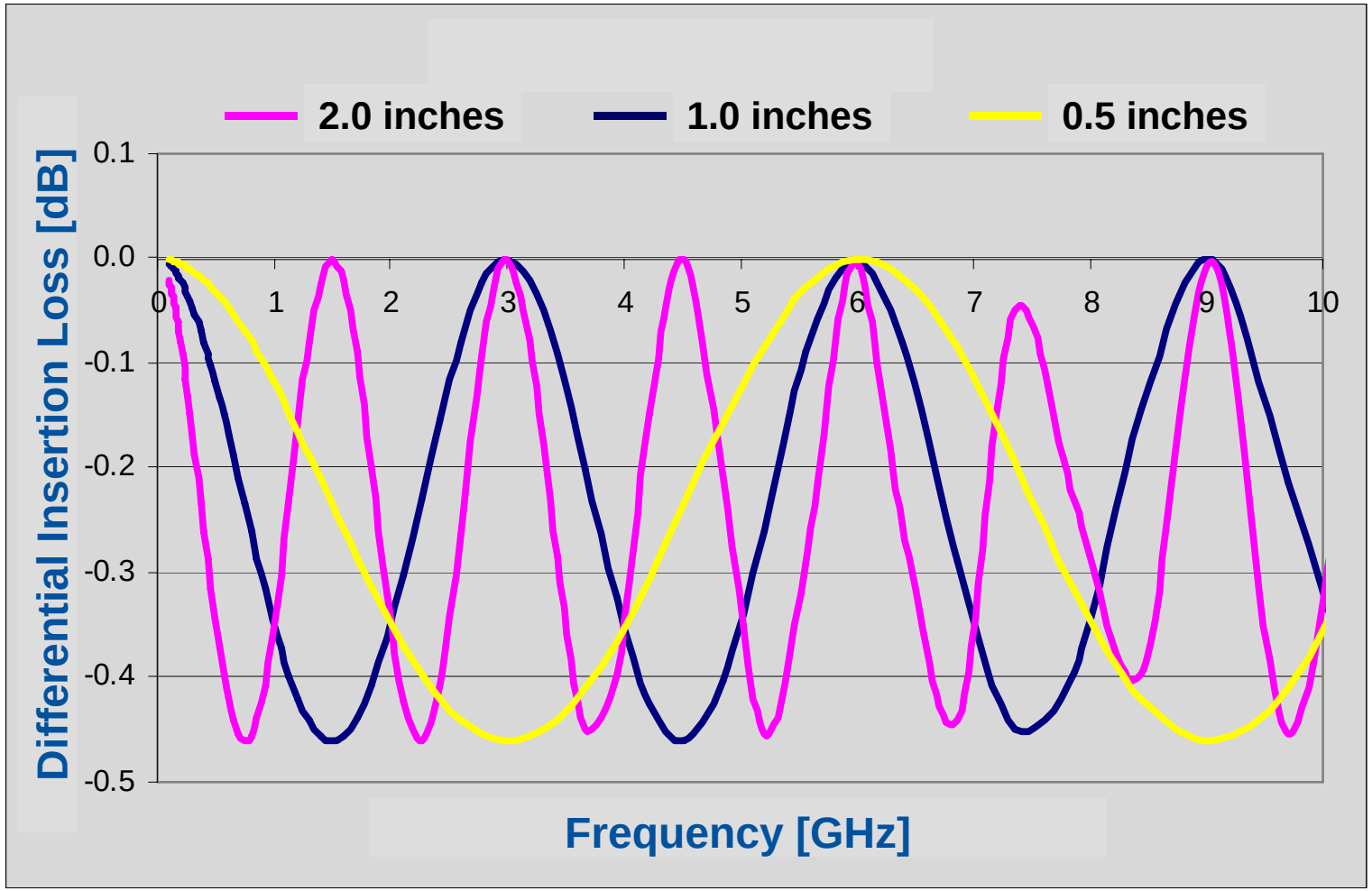
Connectors

- A closer look at connectors shows that even a perfect, lossless, pipe can introduce loss and large amounts of jitter if impedance matching is off.
- The amount of jitter produced is a function of impedance mismatch and of connector length.

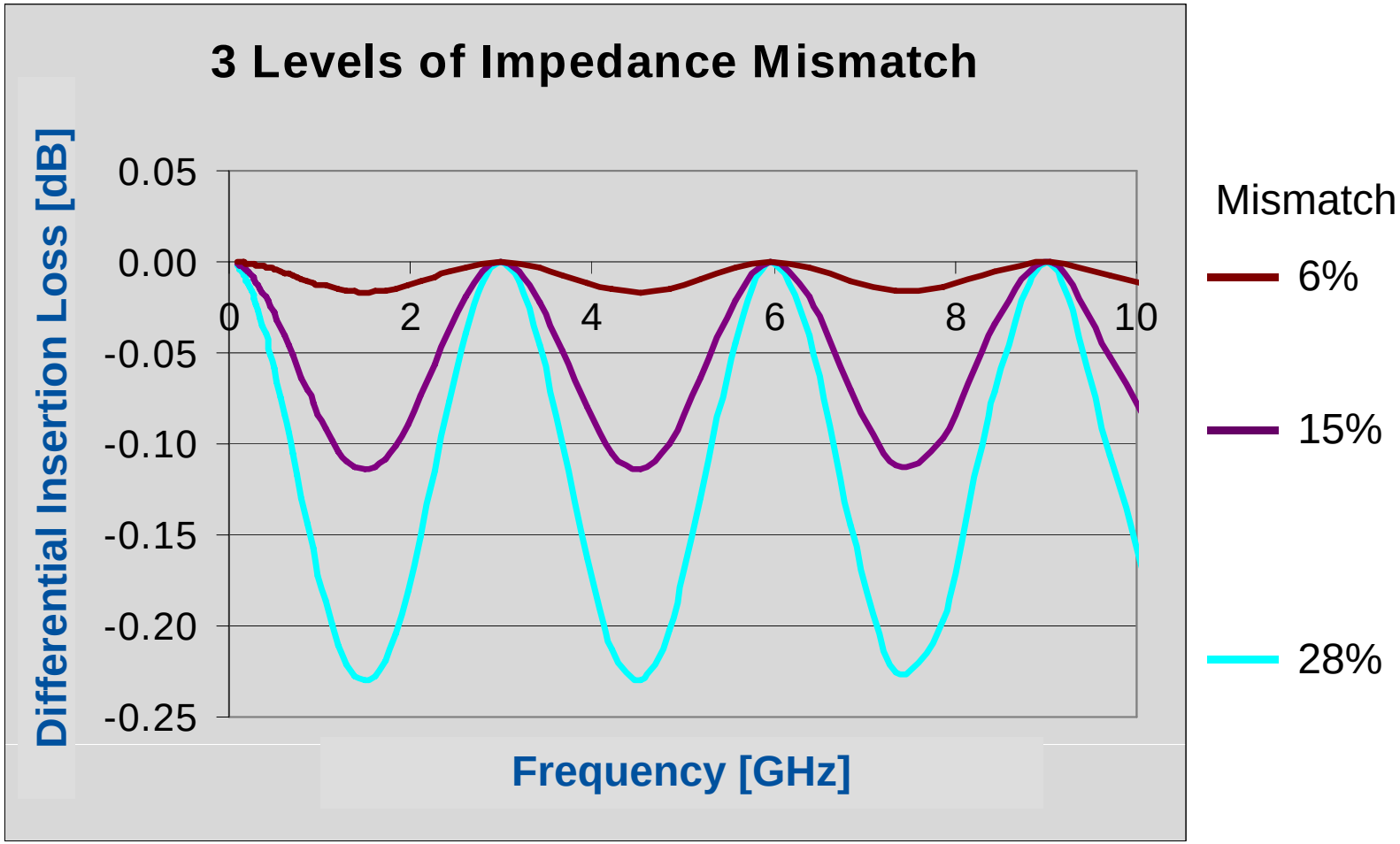
Ideal Connector Model



Ideal Connector's Loss vs. Connector Length



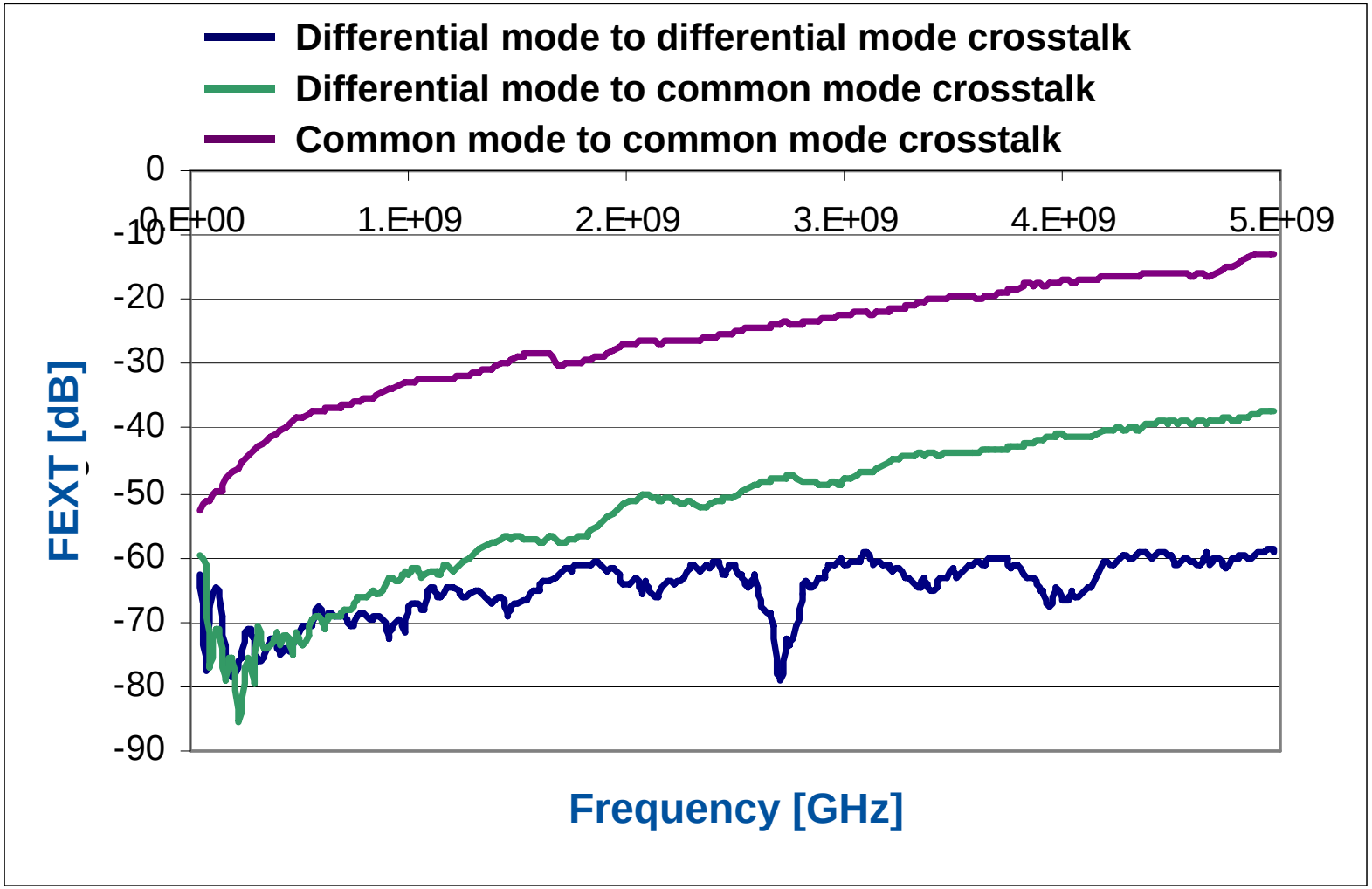
Ideal Connector's Loss vs. Impedance Mismatch



Crosstalk

- On the circuit board options exist for controlling crosstalk:
  - Trace separation
  - Shielding
  - Layer choices
- In connectors, choices are more restrictive:
  - Signal density
  - Connector selection
  - Phase matching control

Typically Common Mode Crosstalks Much Worse Than Differential



In designing a high-speed interconnect circuit, the choice of connector is one of the most serious and unforgiving decisions the engineer must make.

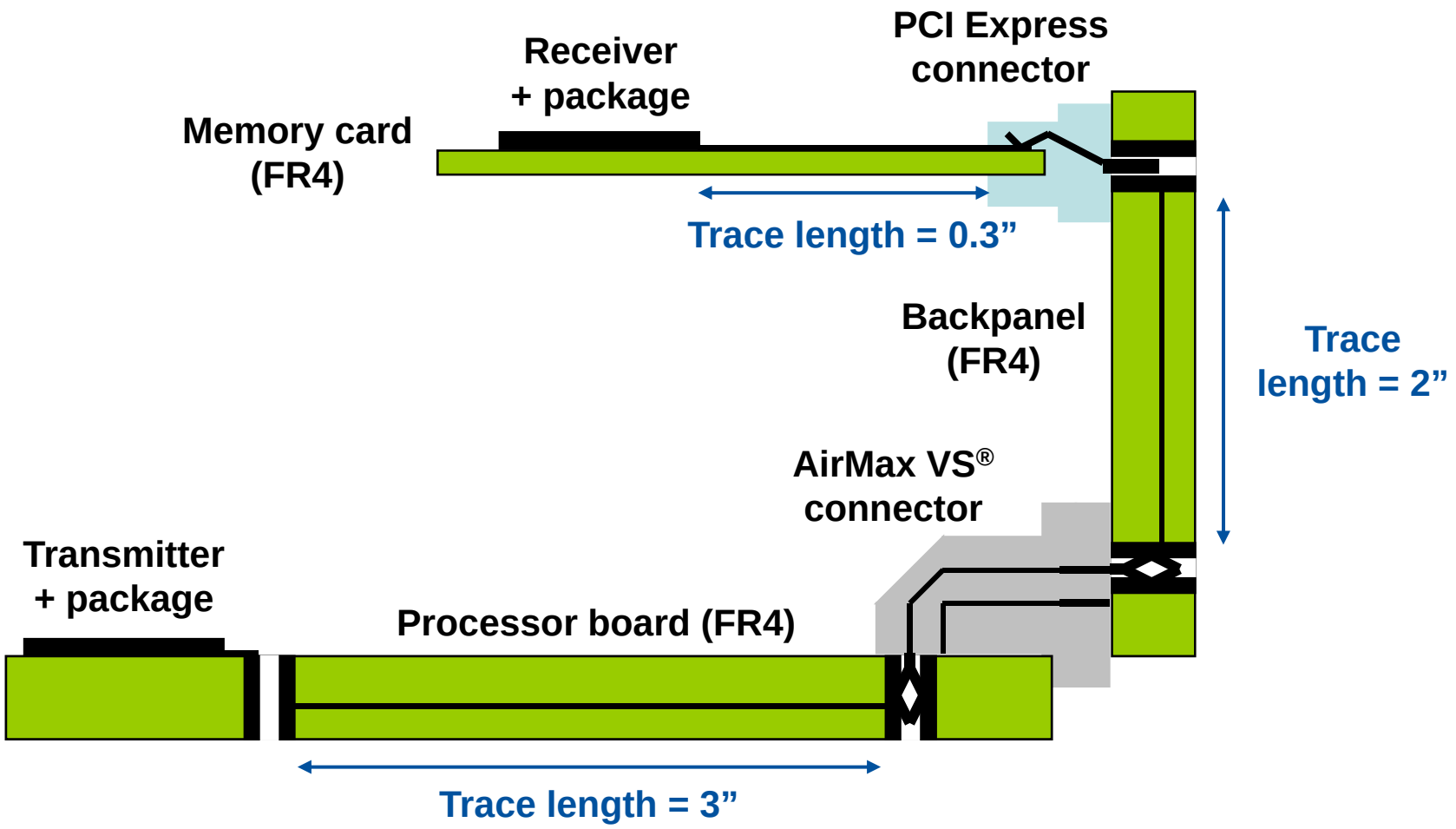
Choose wisely.

Simulated/measured data 85 Ohm links

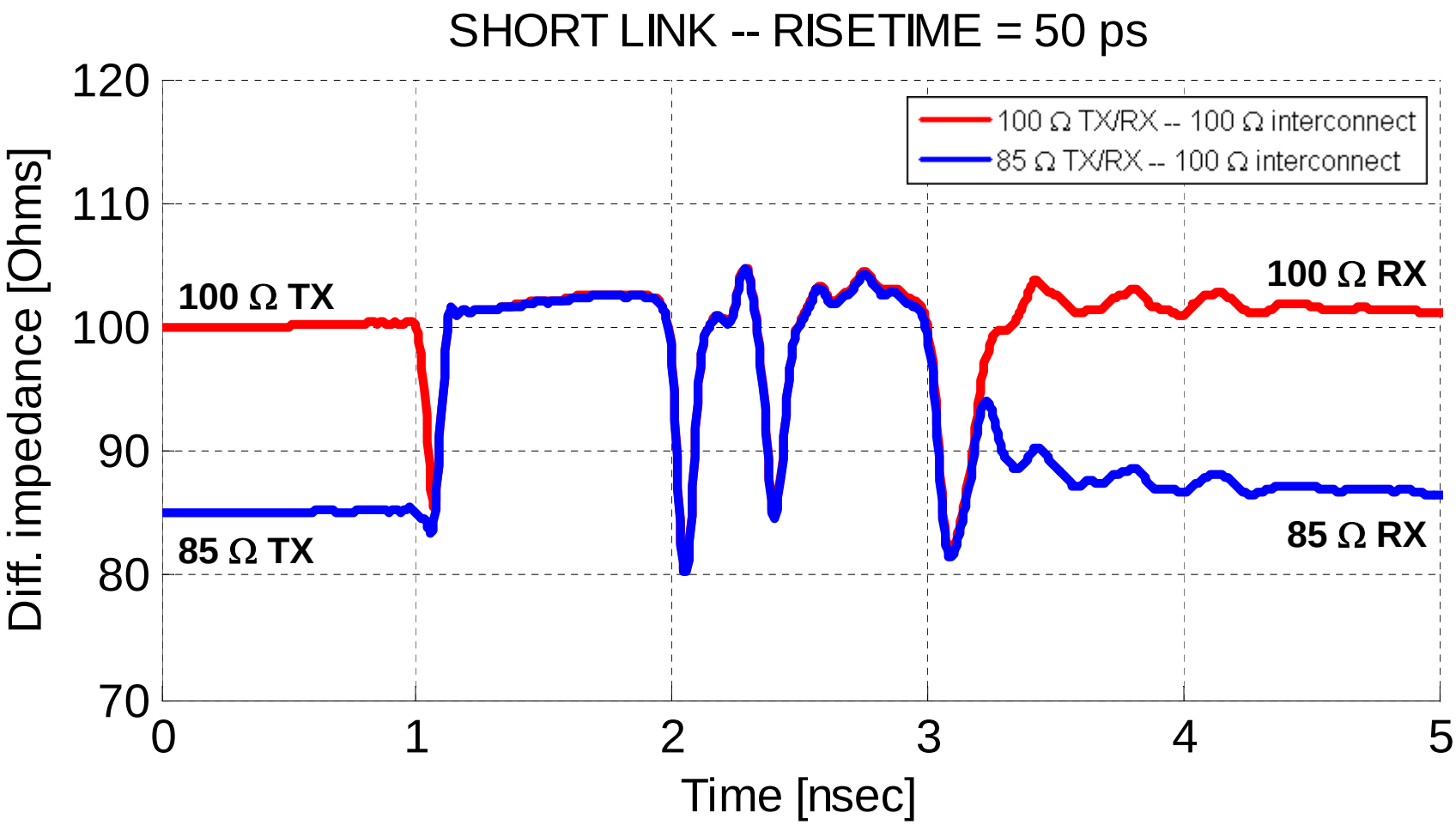
- Switch from 100 Ohm to 85 Ohms packages because of lower loss
  - What does this mean for the interconnection link ?
- Simulation results
  - Server application
  - Backpanel link
- Measurement results
  - Backpanel link

Larger output swing out of 85 Ohm package not included in results

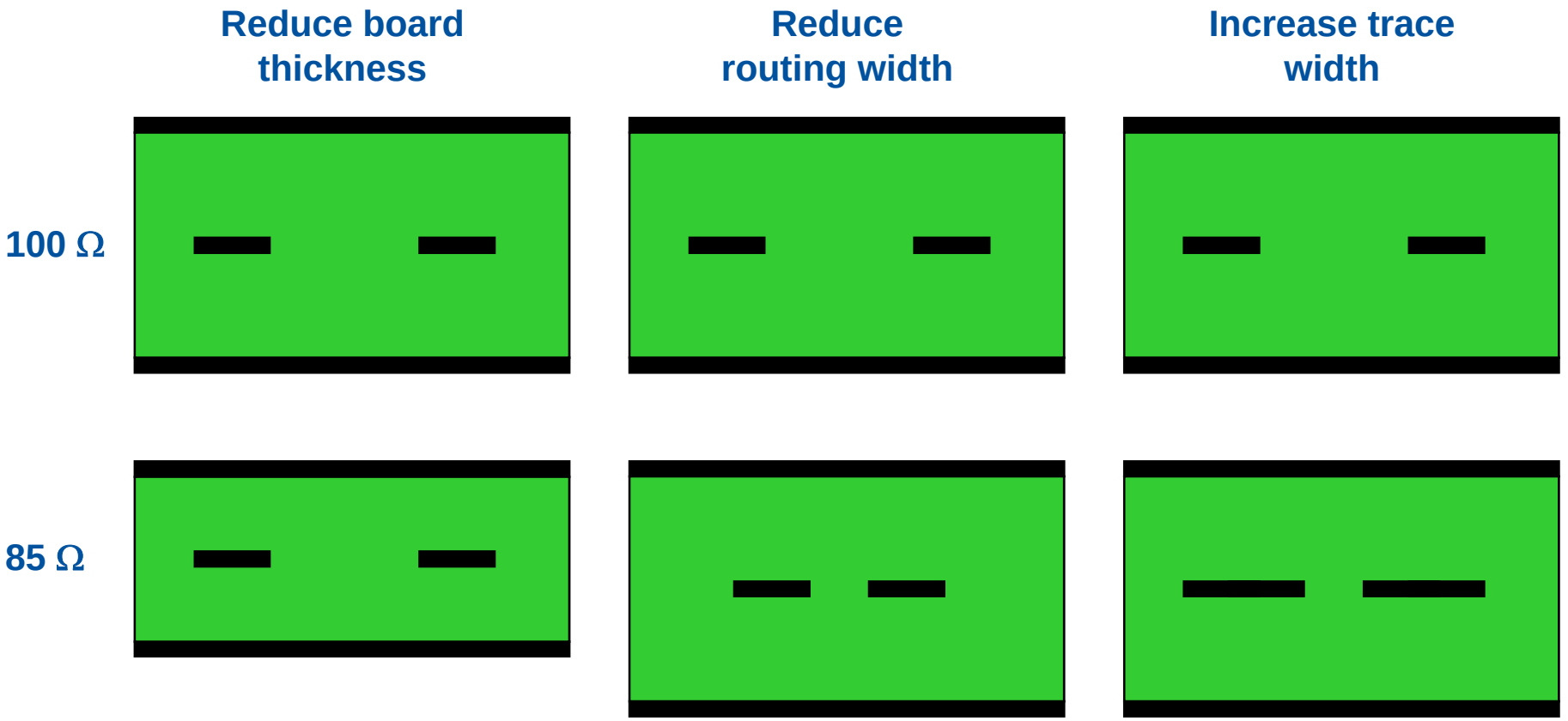
Build-up for Typical Server Application



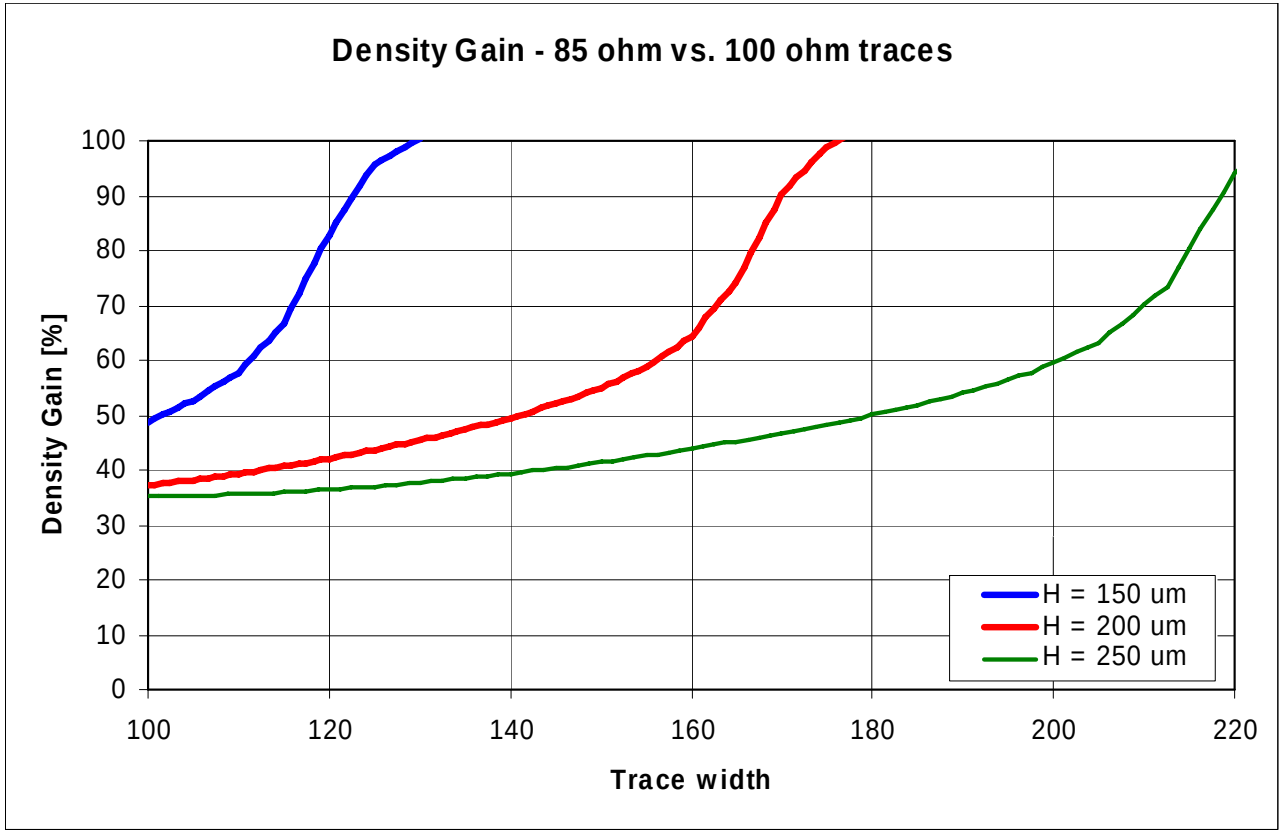
Impedance Profile

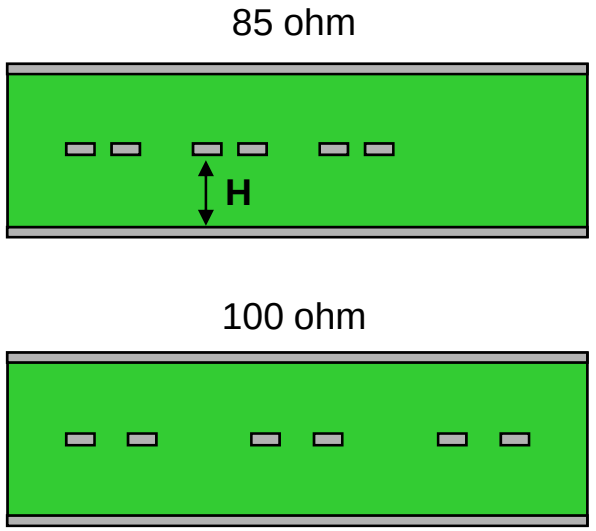


Lowering Board Impedance



Density Increase



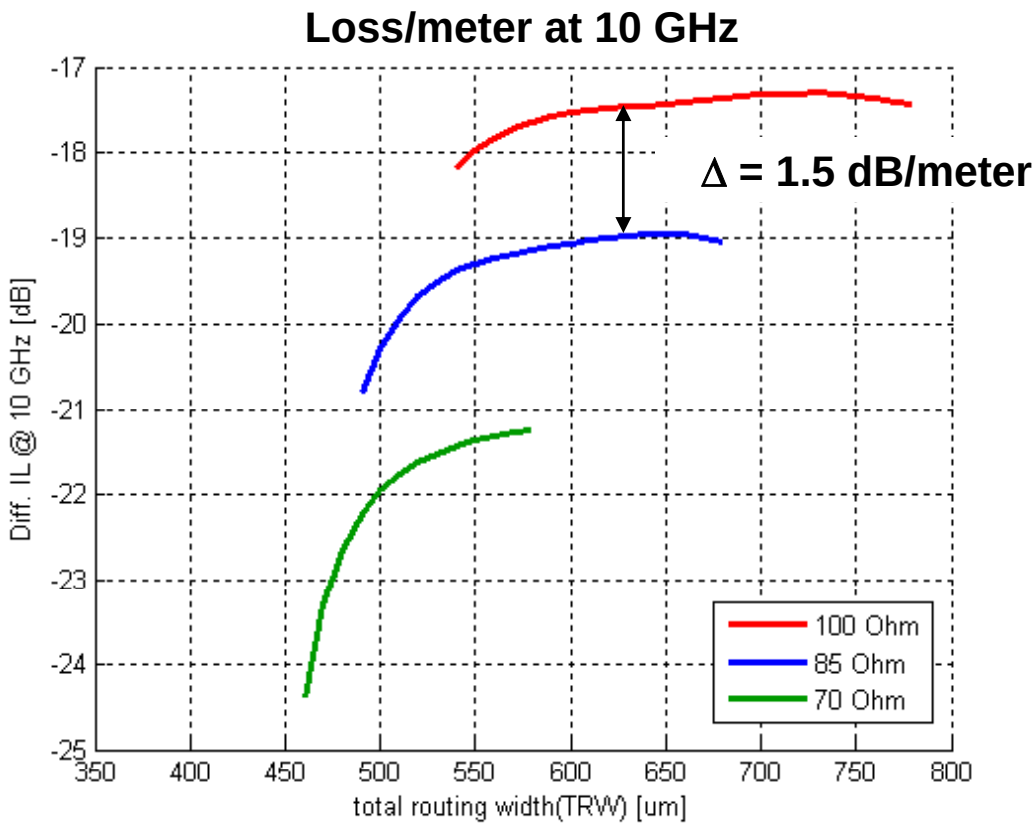


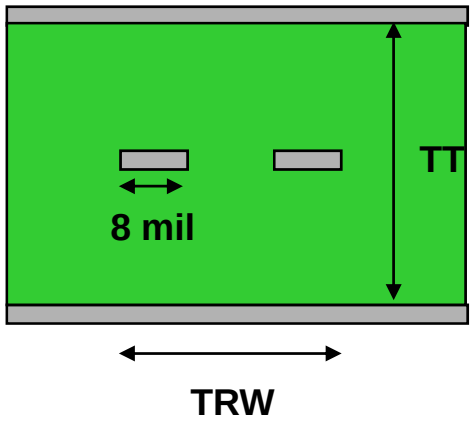
Assumption: Pair to pair isolation
= 3 x trace to trace isolation

$$\text{Density Gain} = 100 \frac{Nr\ 85\,\Omega\ pairs/cm}{Nr\ 100\,\Omega\ pairs/cm} - 100$$

PCB Losses

- Loss of a 85 Ω trace > loss of a 100 Ω trace

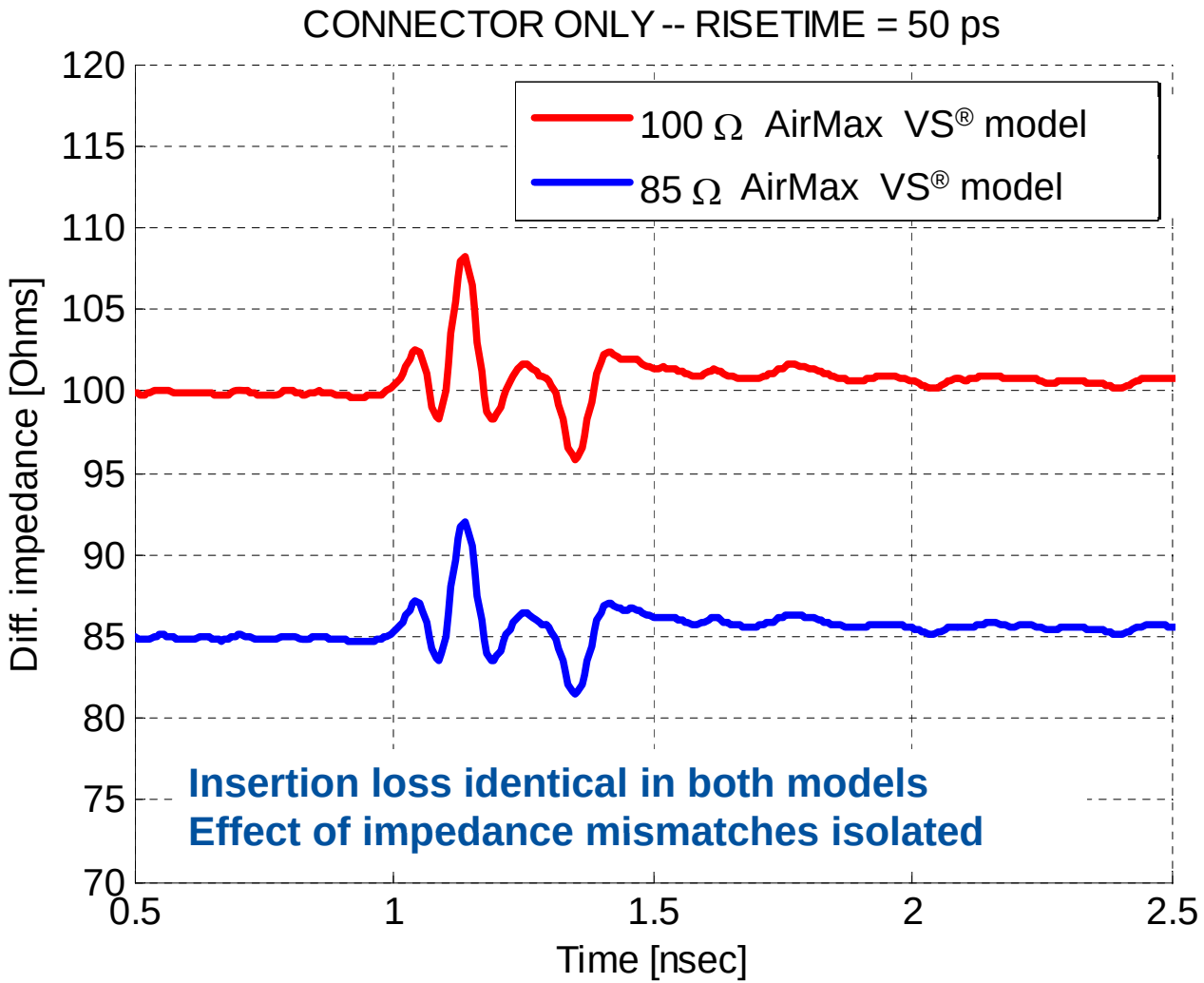




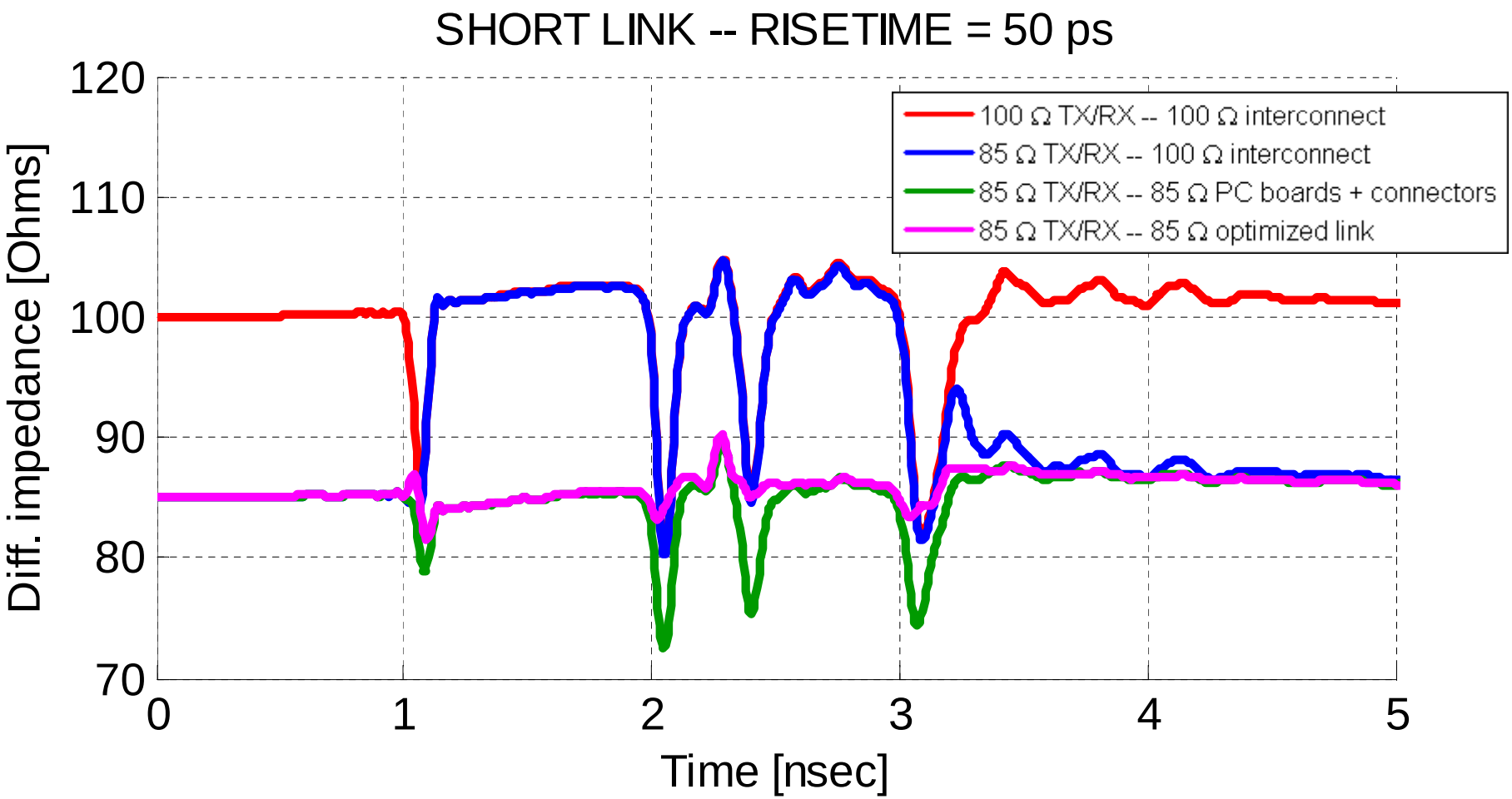
Trace width = 200 um
Trace thickness = 18 um
Dielectric constant = 3.5
Loss tangent = 0.005

- Disadvantage limited for short links (function of build-up and layout)

85 Ohms AirMax VS® connector model

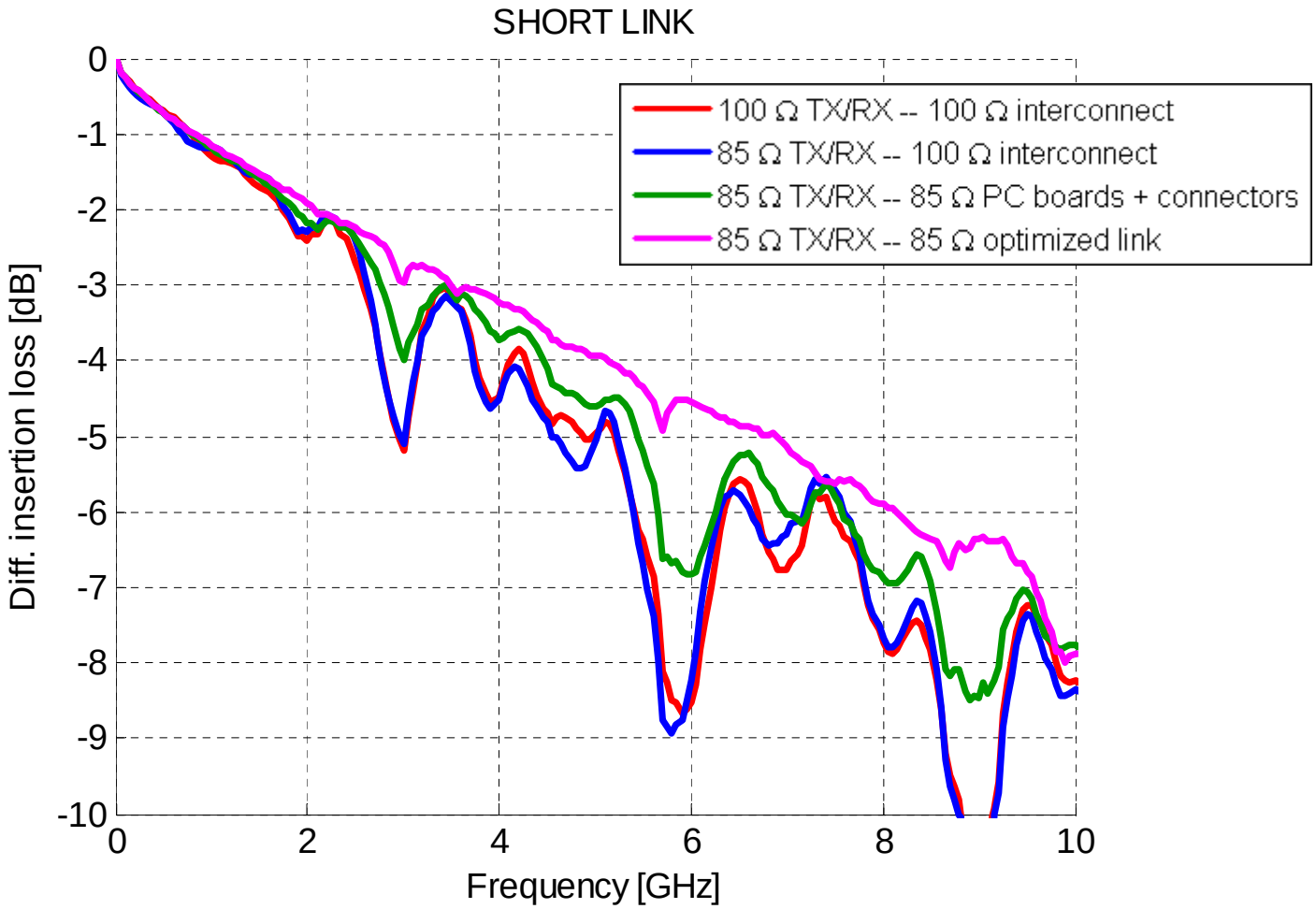


Impedance Profile

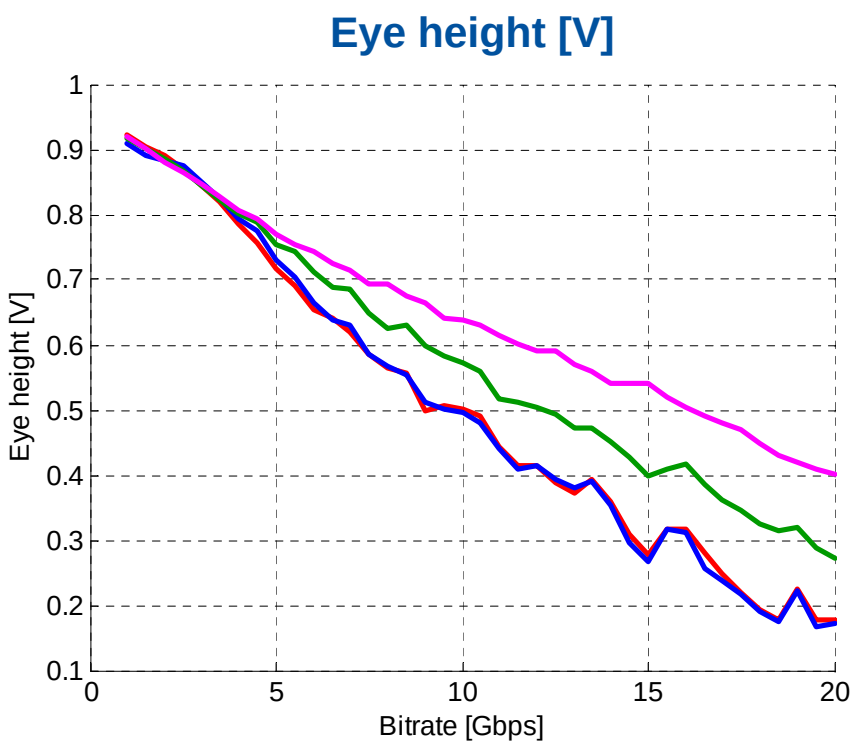


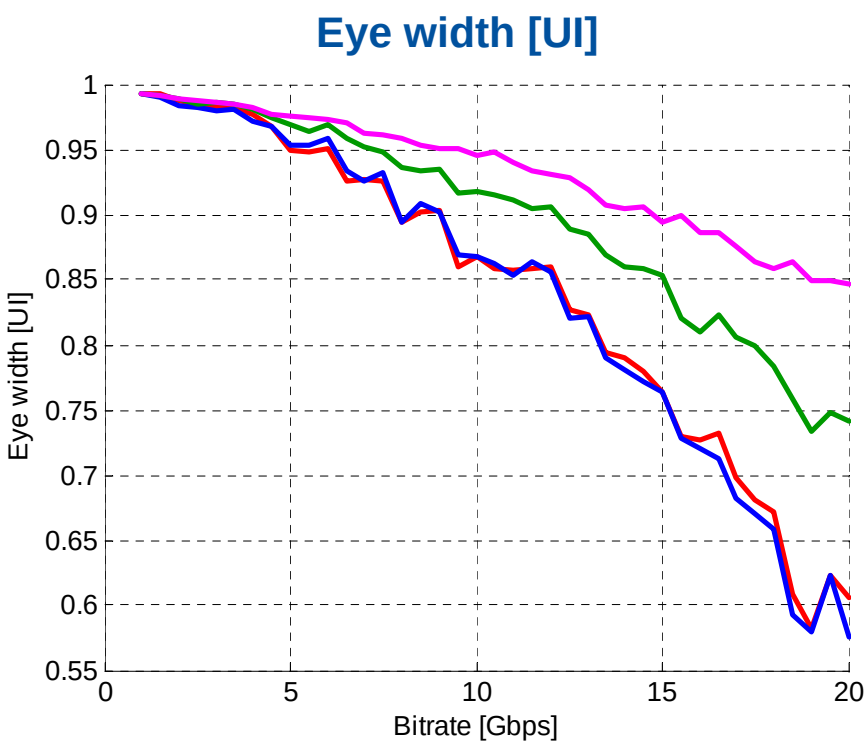
"85 Ω optimized" link is with optimized vias, other links are with standard vias

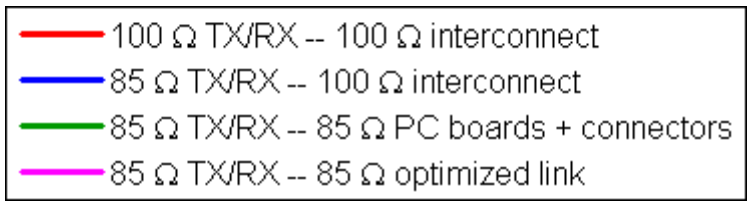
Insertion Loss



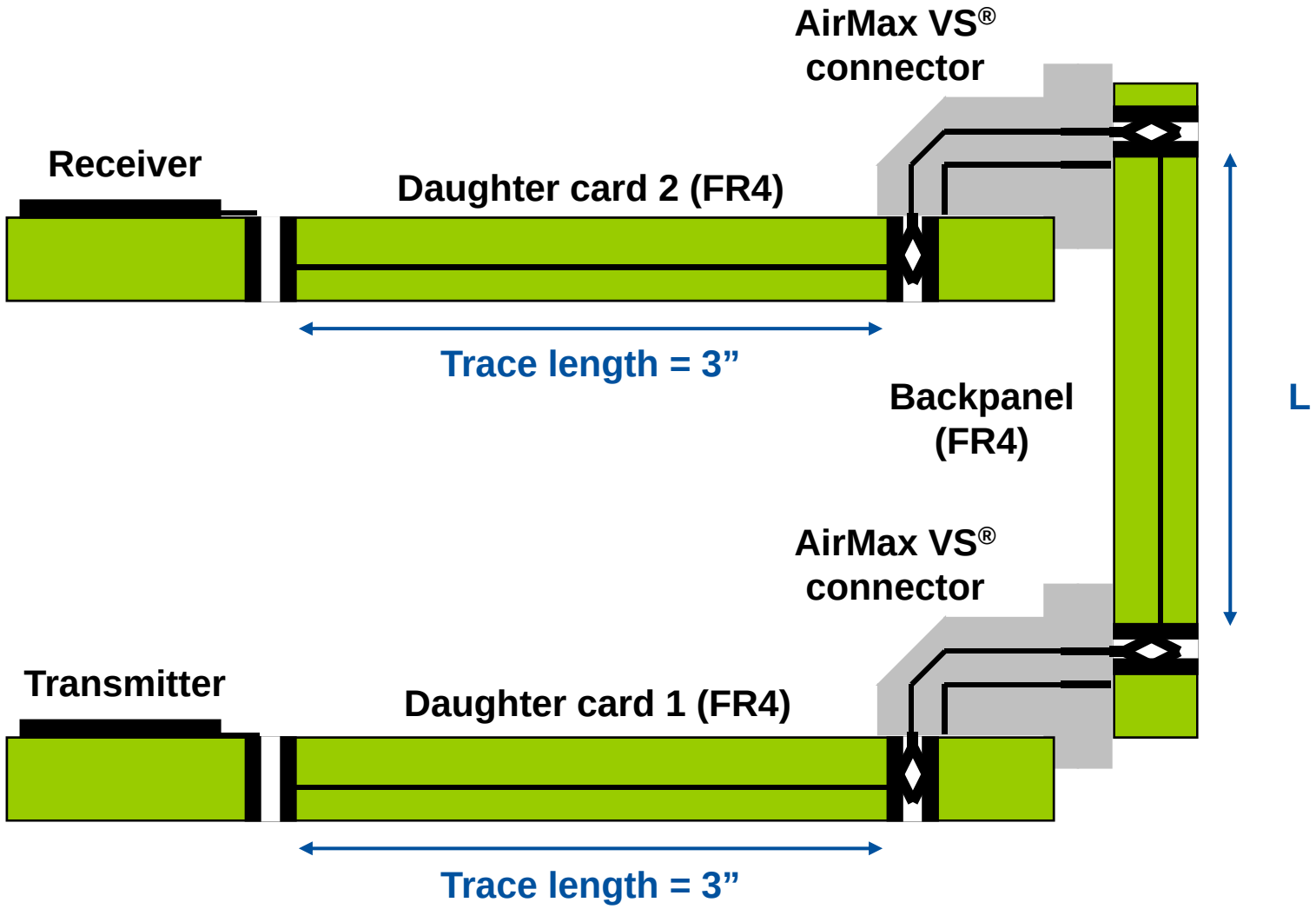
Eye Opening vs. Bitrate



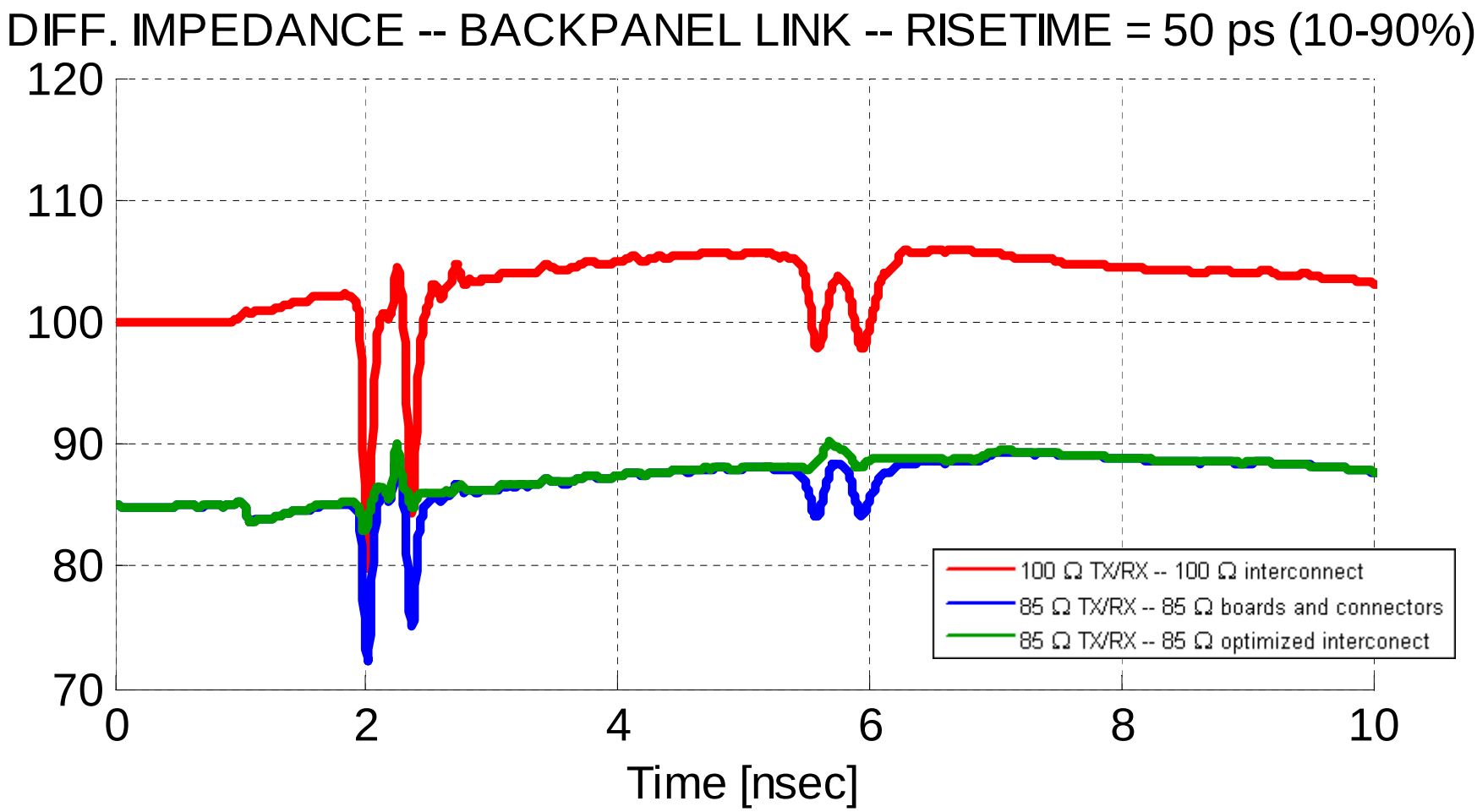




Build-up Backpanel Link



Impedance Profile – 16” Link



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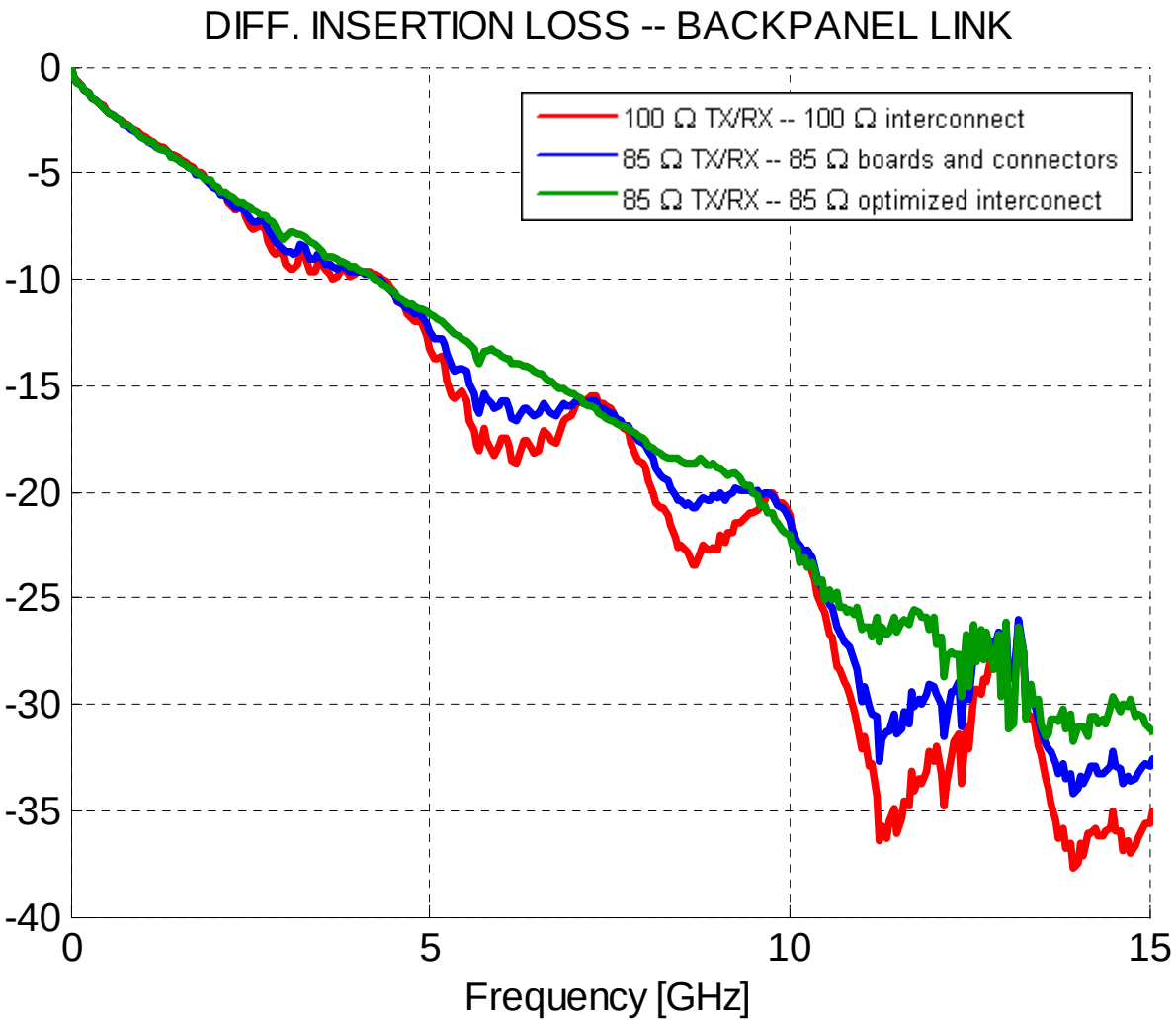
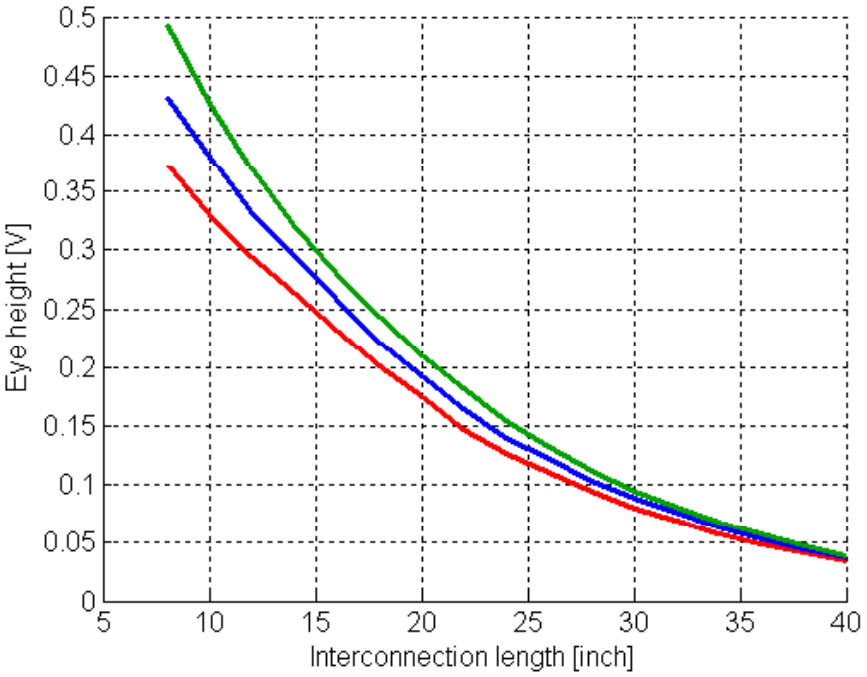
Insertion Loss – 16” Link

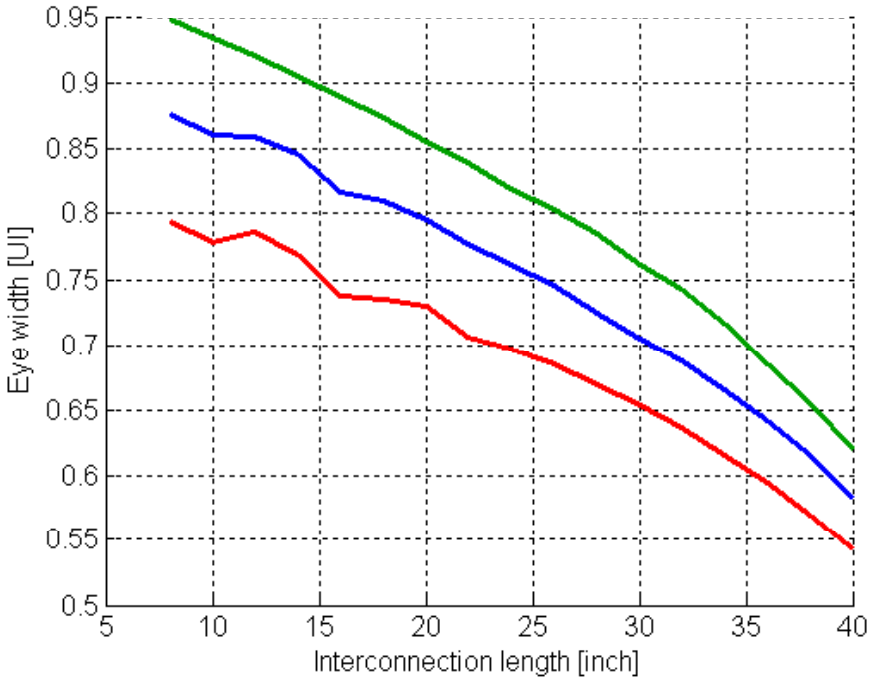


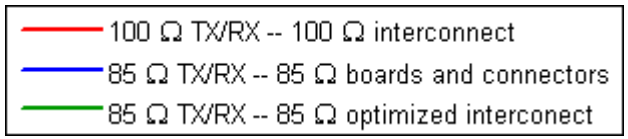
Eye Opening vs. Length – 10 GBPS – 4-taps DE

Eye height [V]



Eye width [UI]

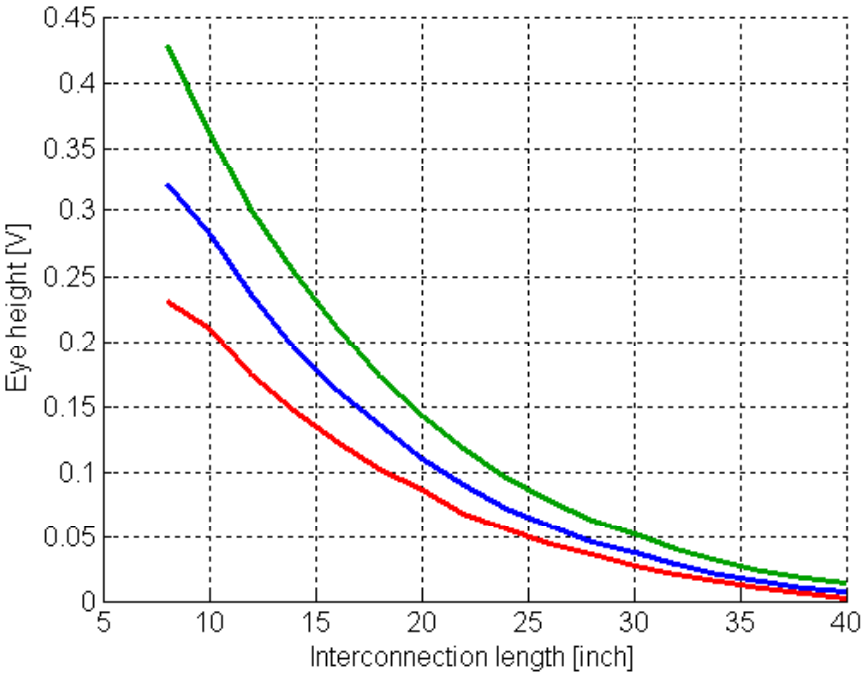




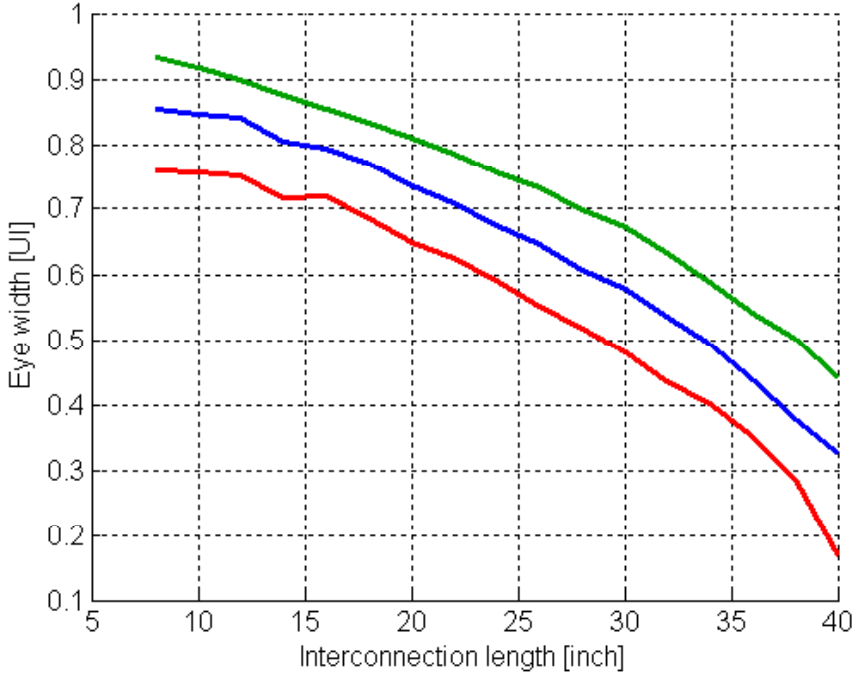
1 pre-cursor
2 post-cursors

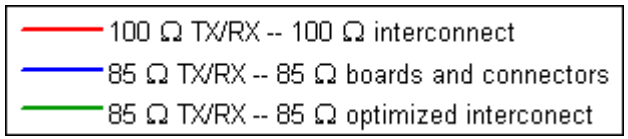
Eye Opening vs. Length – 12.5 GBPS – 4-taps DE

Eye height [V]



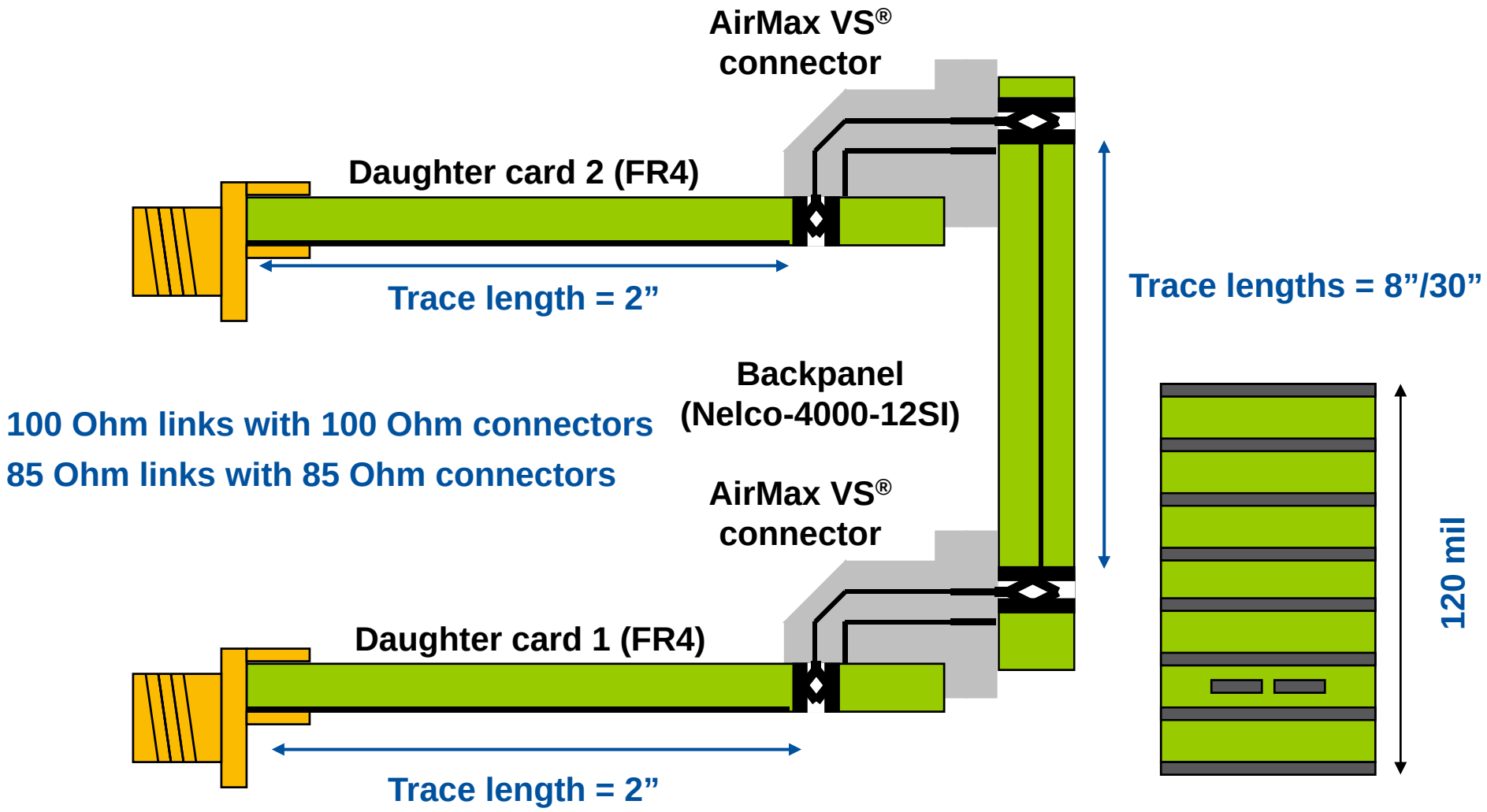
Eye width [UI]



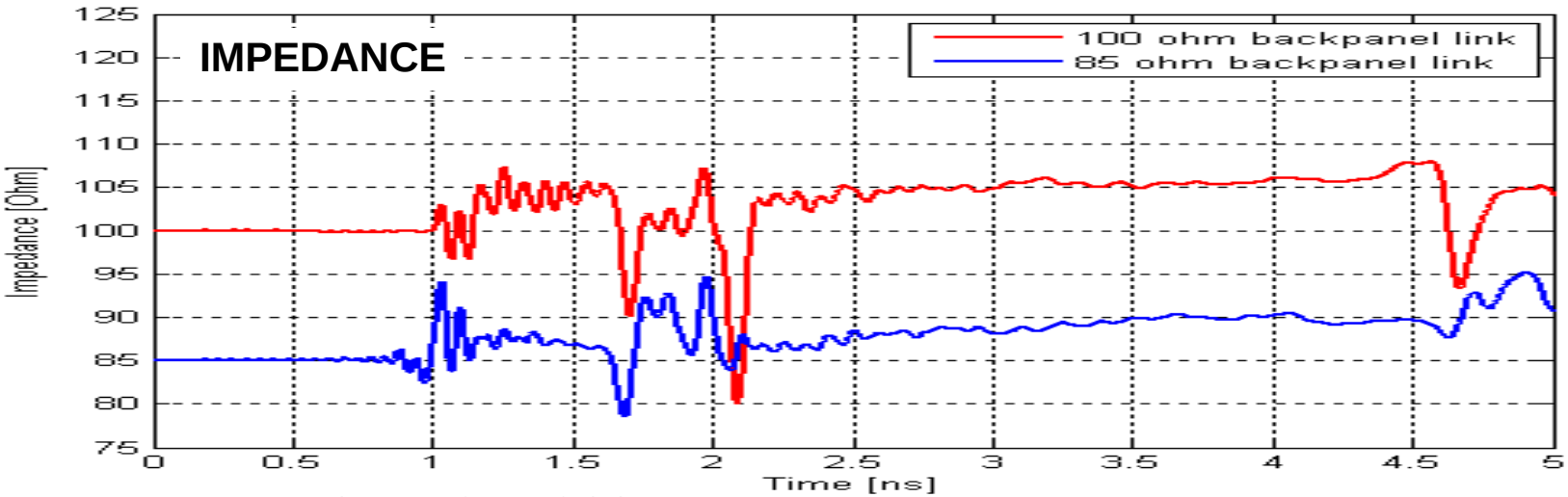


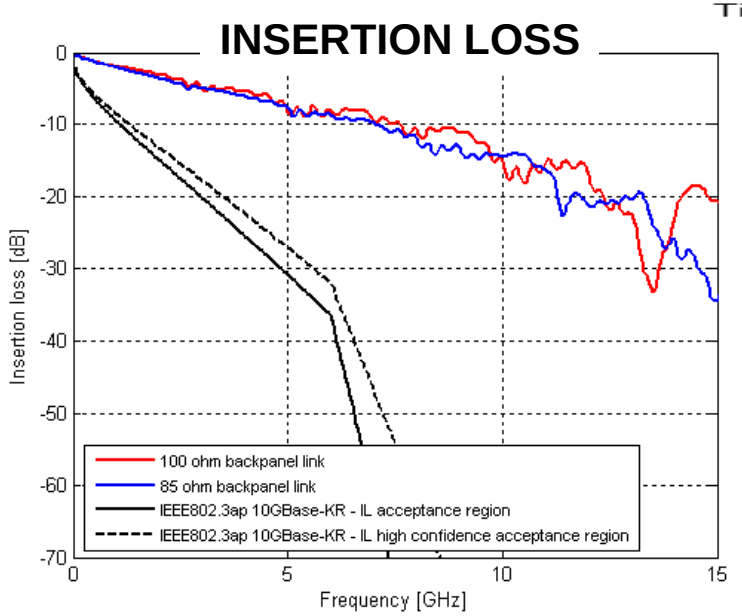
1 pre-cursor
2 post-cursors

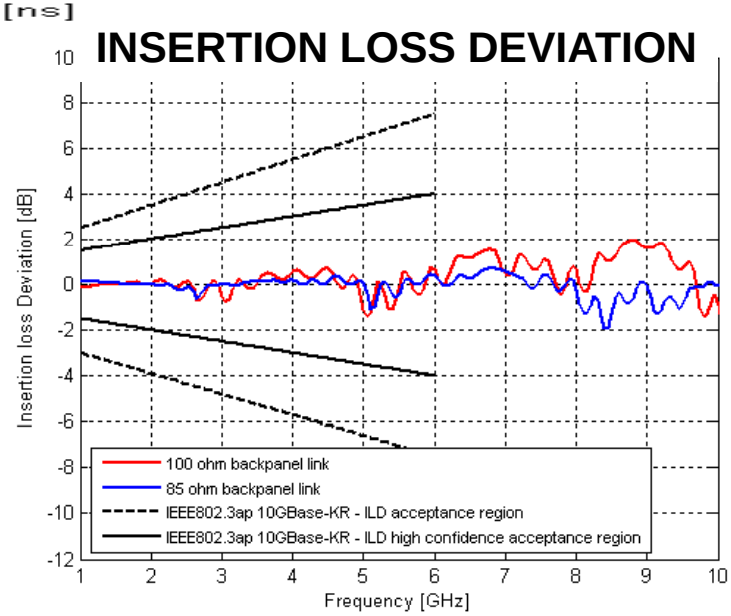
Measurements Demonstrator



Backpanel length = 8″

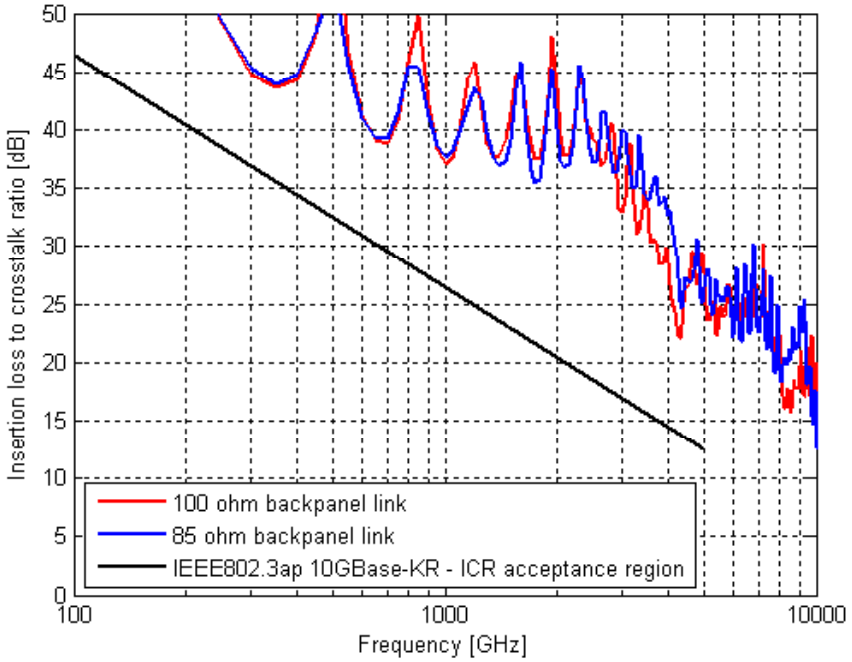




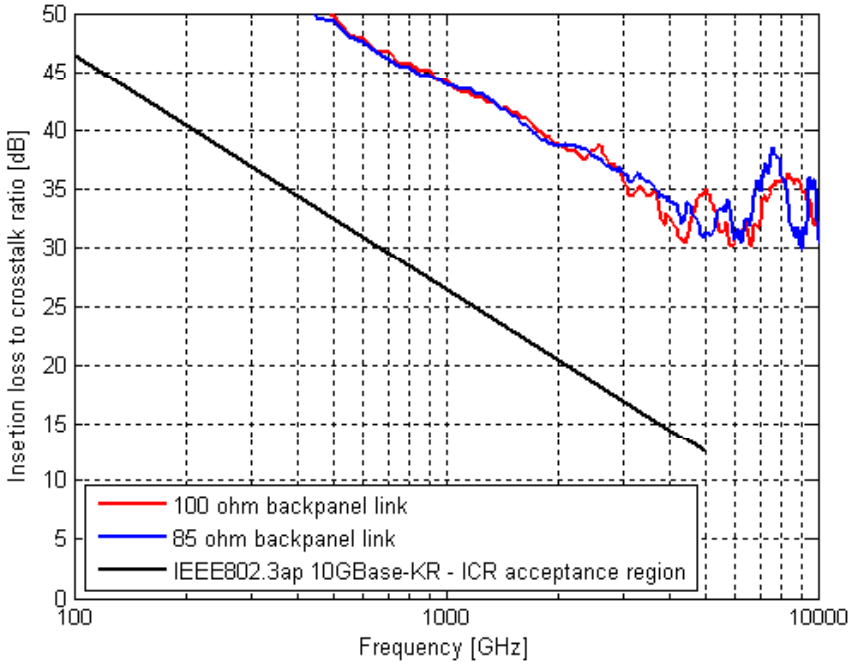


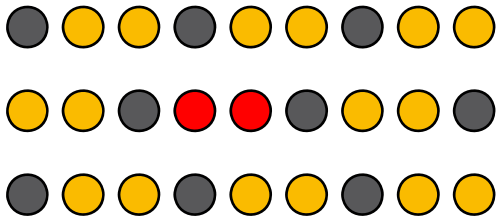
Backpanel length = 8˝

IL TO XT RATIO: NEXT



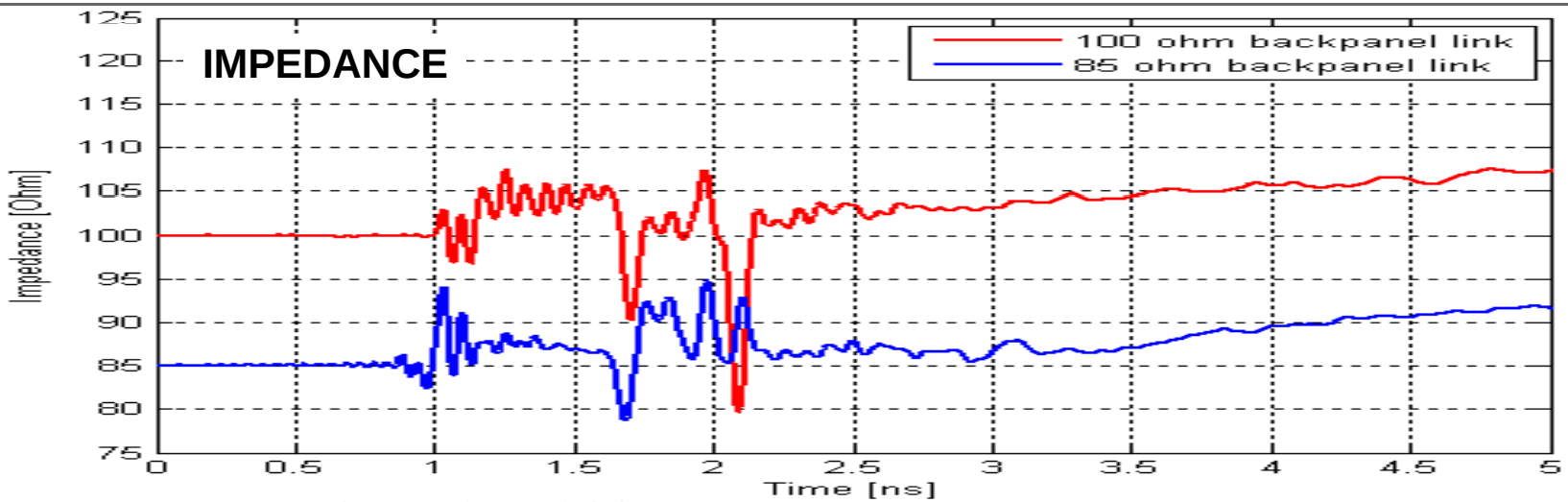
IL TO XT RATIO: FEXT

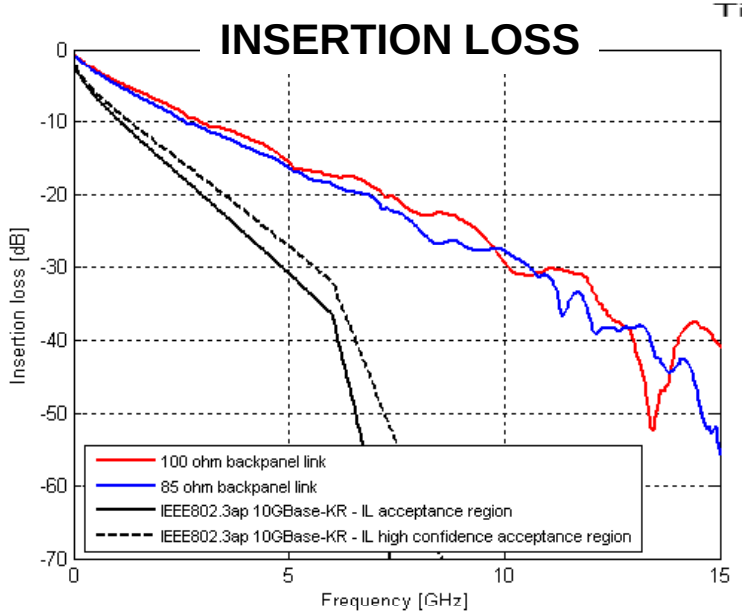


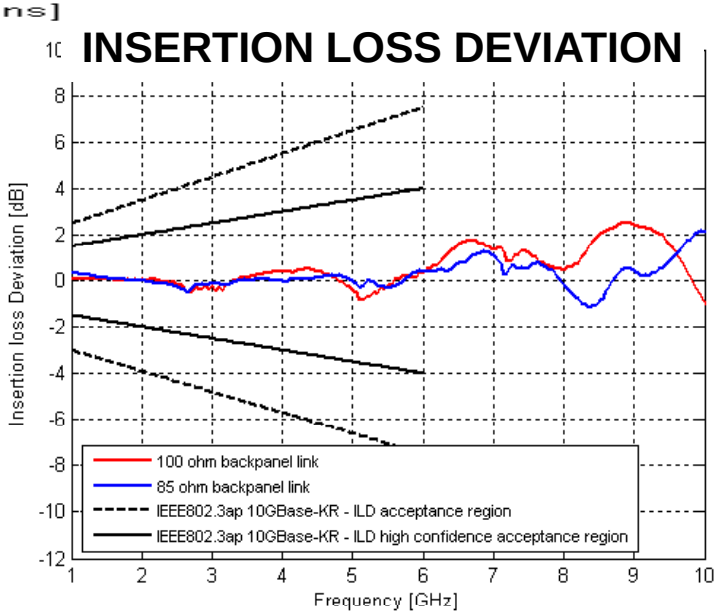


Cross-talk on a victim pair generated by 8 aggressor pairs

Backpanel length = 30″

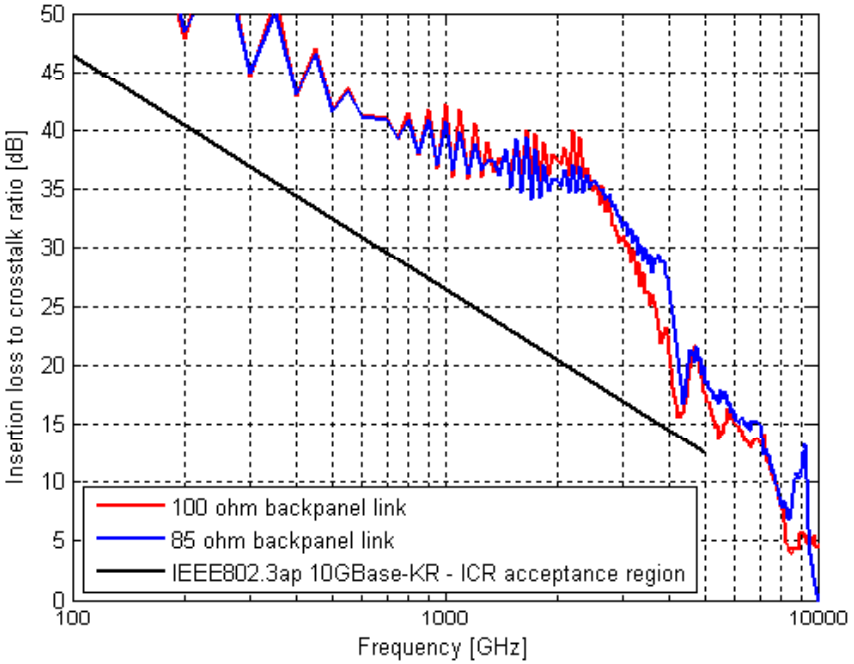




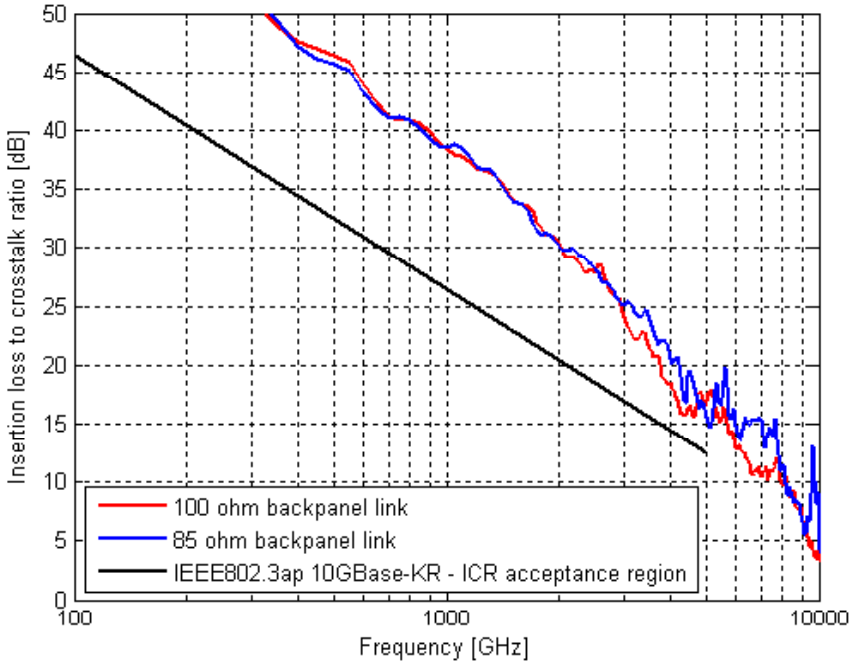


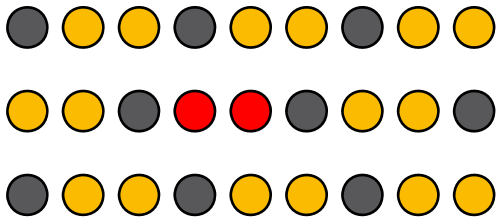
Backpanel length = 30˝

IL TO XT RATIO: NEXT



IL TO XT RATIO: FEXT





Cross-talk on a victim pair generated by 8 aggressor pairs

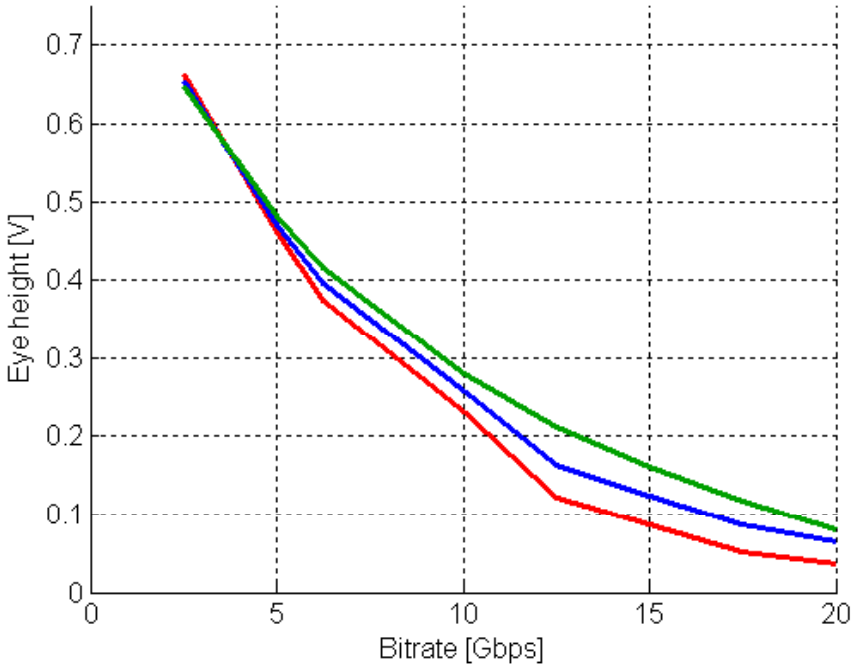
Conclusions

- 85 Ohms package less loss than 100 Ohm package
- Match interconnection link impedance to 85 Ohms TX/RX
  - Reduce impedance mismatches
  - Easier to design (PF) via holes for 85 Ohm than for 100 Ohm
  - Smoother IL curve (signal conditioning efficiency)
  - Most effective for non-loss dominated links: short links, low loss materials
- Other effects
  - Density gain
  - Reduced board thickness: material/cost reduction
- PCB losses
  - 85 Ohm boards higher losses than 100 Ohm boards
  - Compensated by larger output swing out of 85 Ohm package

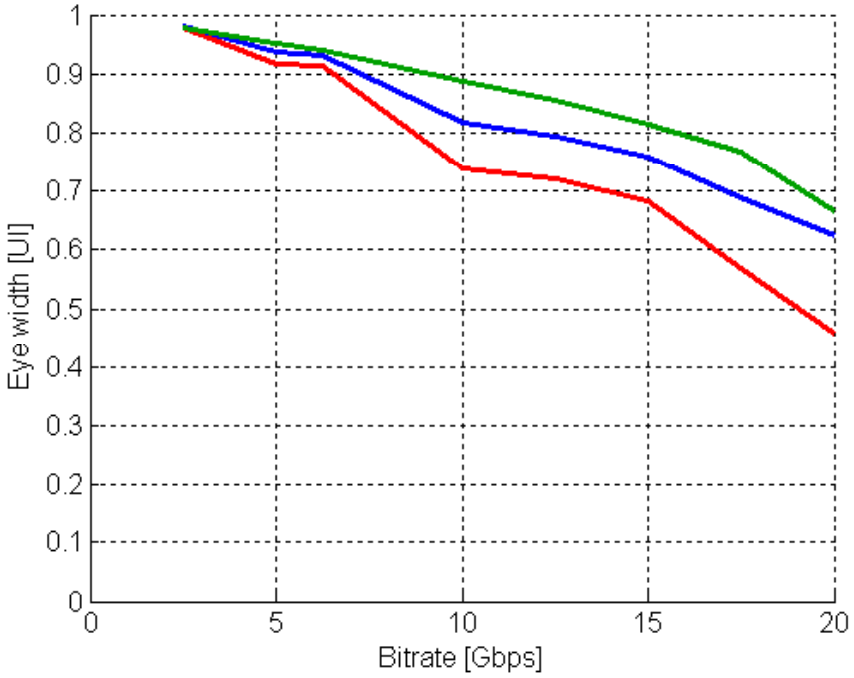
Questions

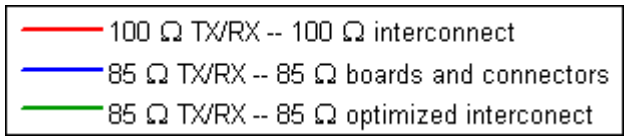
Eye Opening vs. Bitrate – 16” Link – 4-taps DE

Eye height [V]



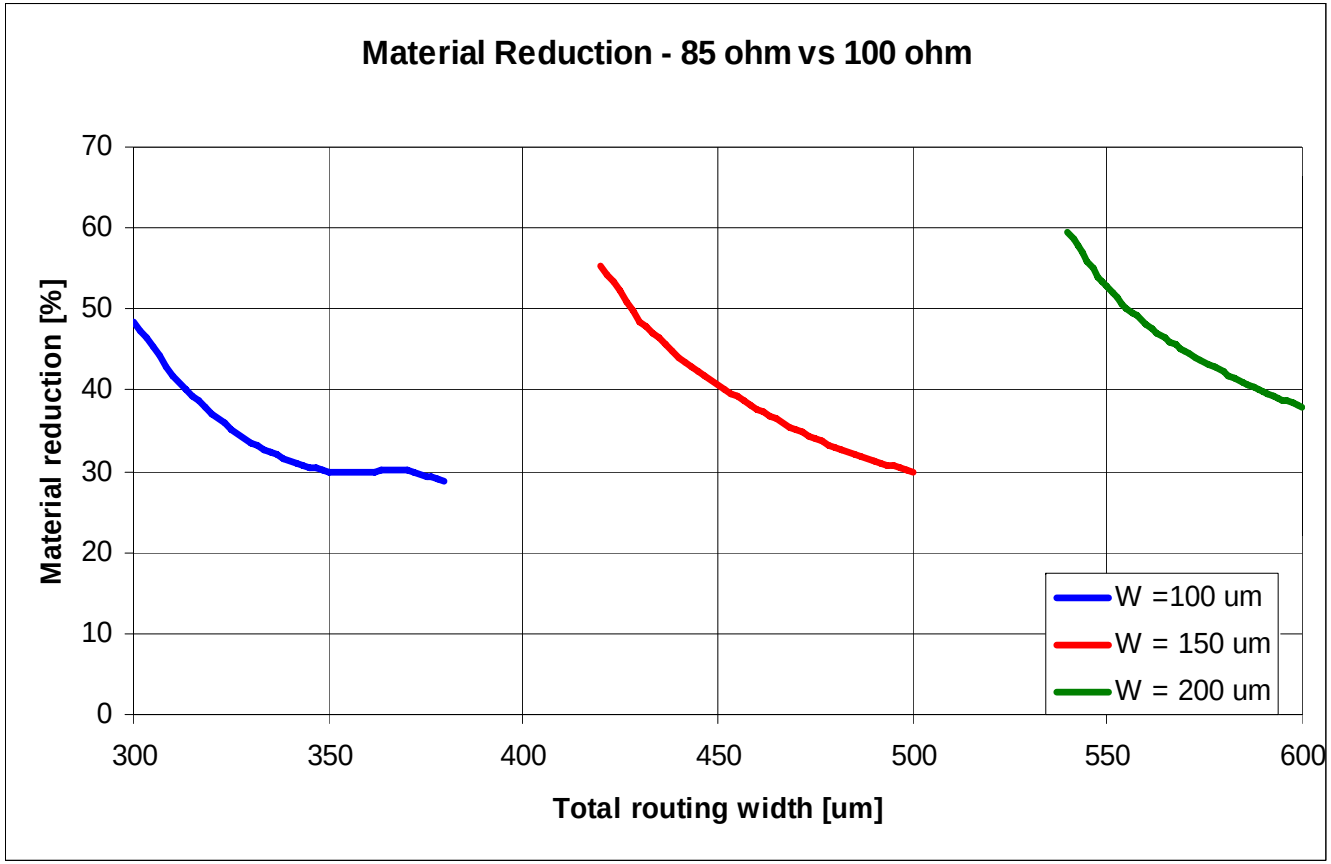
Eye width [UI]

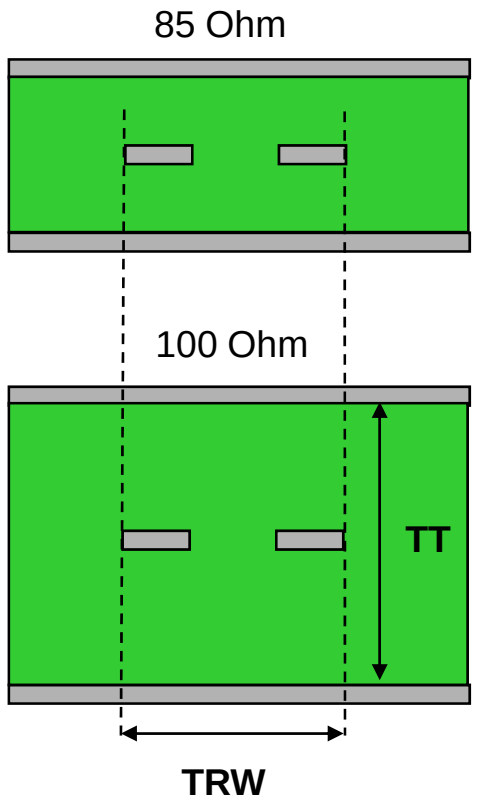




1 pre-cursor
2 post-cursors

Material/Cost Reduction





$$\text{Material Reduction} = 100 - 100\frac{TT_{85ohm}}{TT_{100ohm}}$$