

Customer Simulation Report:

BergStak[®] 0.8mm Mezzanine Connectors

SMT Vertical Header to SMT Vertical Receptacle

8mm PCB Stack Height

Part Numbers: 61083, 61082

vs. PCIe[®] Gen 2, 3

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- This document shows the electrical performance of the BergStak[®] 0.8mm Mezzanine Connector System in a 8mm stack height configuration compared against the PCIe[®] Gen 2 Specifications.
 - Spec limit lines are shown on the plots of relevant electrical parameters:
 - Return Loss (R.L.)
 - Insertion Loss (I.L.)
 - Near-End Crosstalk (NEXT)
 - Shown are the results for this wiring pattern:
 - GSSGSSG

- BergStak® 0.8mm Mezzanine connectors , with a stack height of 8mm using this wiring pattern, meet the return loss, insertion loss and cross talk requirements of PCIe® Gen 2.

Application Notes

- Shorter stack heights will perform better, as the crosstalk resonance will move higher in frequency.
- Higher stack heights will perform worse, as the crosstalk resonance will move lower in frequency.
- This conclusion is re-stated on the final slide.

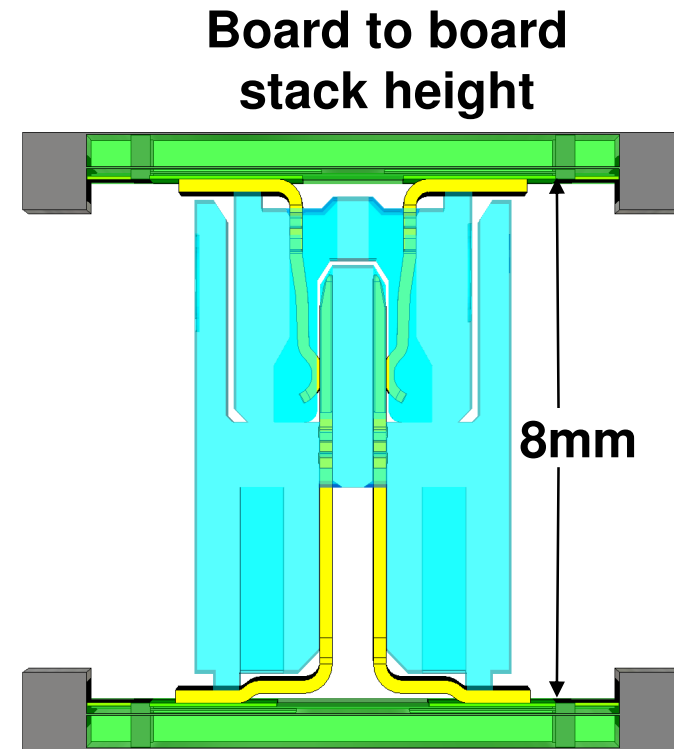
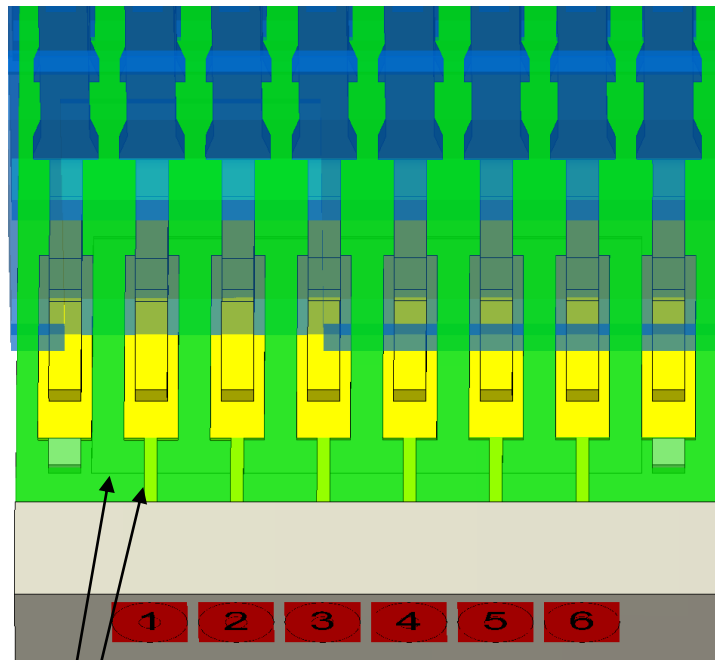
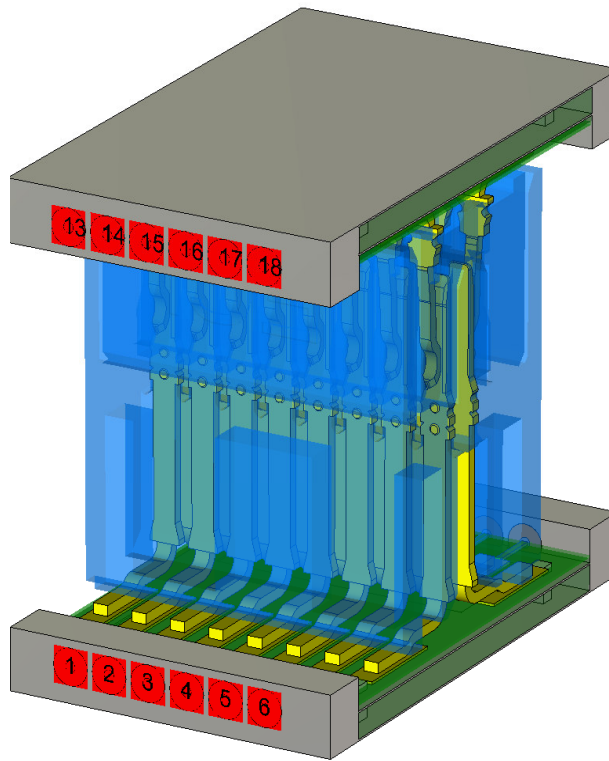
- The specific performance and compliance requirements proposed by the PCIe[®] Gen 3 CEM working group have been reviewed by FCI.
- Information shown in this report for PCIe[®] Gen 2 is compatible with PCIe[®] Gen 3.
- FCI will provide compliance details when PCIe[®] Gen 3 is released to the public

- The Bergstak® solid model was analyzed using CST MicroWave Studio software and the results were post-processed using MATLAB in order to compare the performance against the PCIe® Gen. 2 specification.

- Simulation Details:
 - Tool used: CST MWS
 - Model was run to a maximum frequency of 20 GHz

 - Touchstone file used to generate results:
“bs_8mm_nud_v3_woren_401_0to20.s24p”
 - Model frequency range: d.c. to 20 GHz in increments of 50 MHz (i.e. 401 points)

BergStak[®] 8mm Geometry Modeled



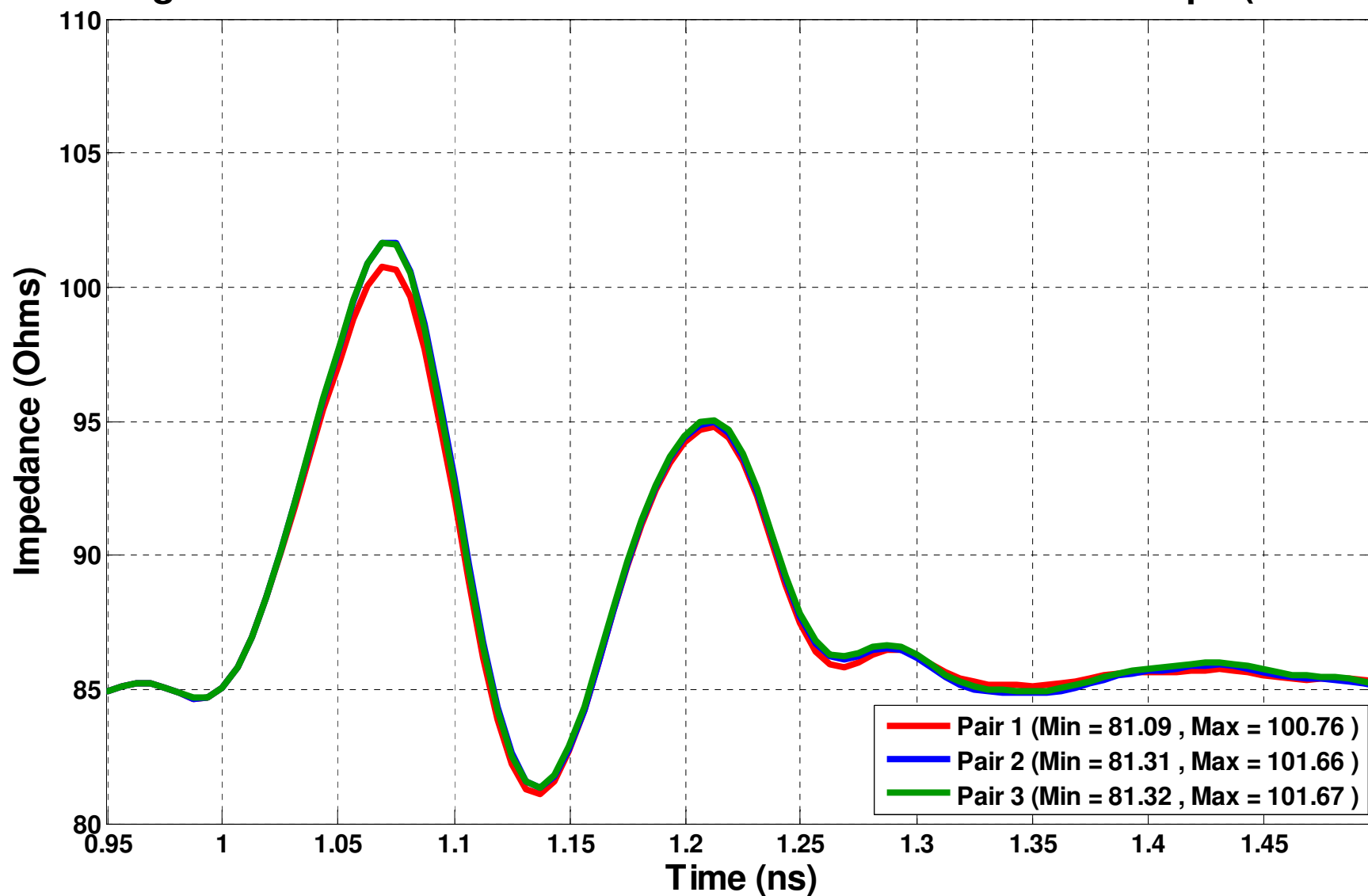
**PNs: 61083 (Vertical SMT Header)
61082 (Vertical SMT Receptacle)**

Note: 1mm of trace before SMT pads and SMT pads with void underneath (impedance control) are included in model and results

Differential Impedance (GSSG)



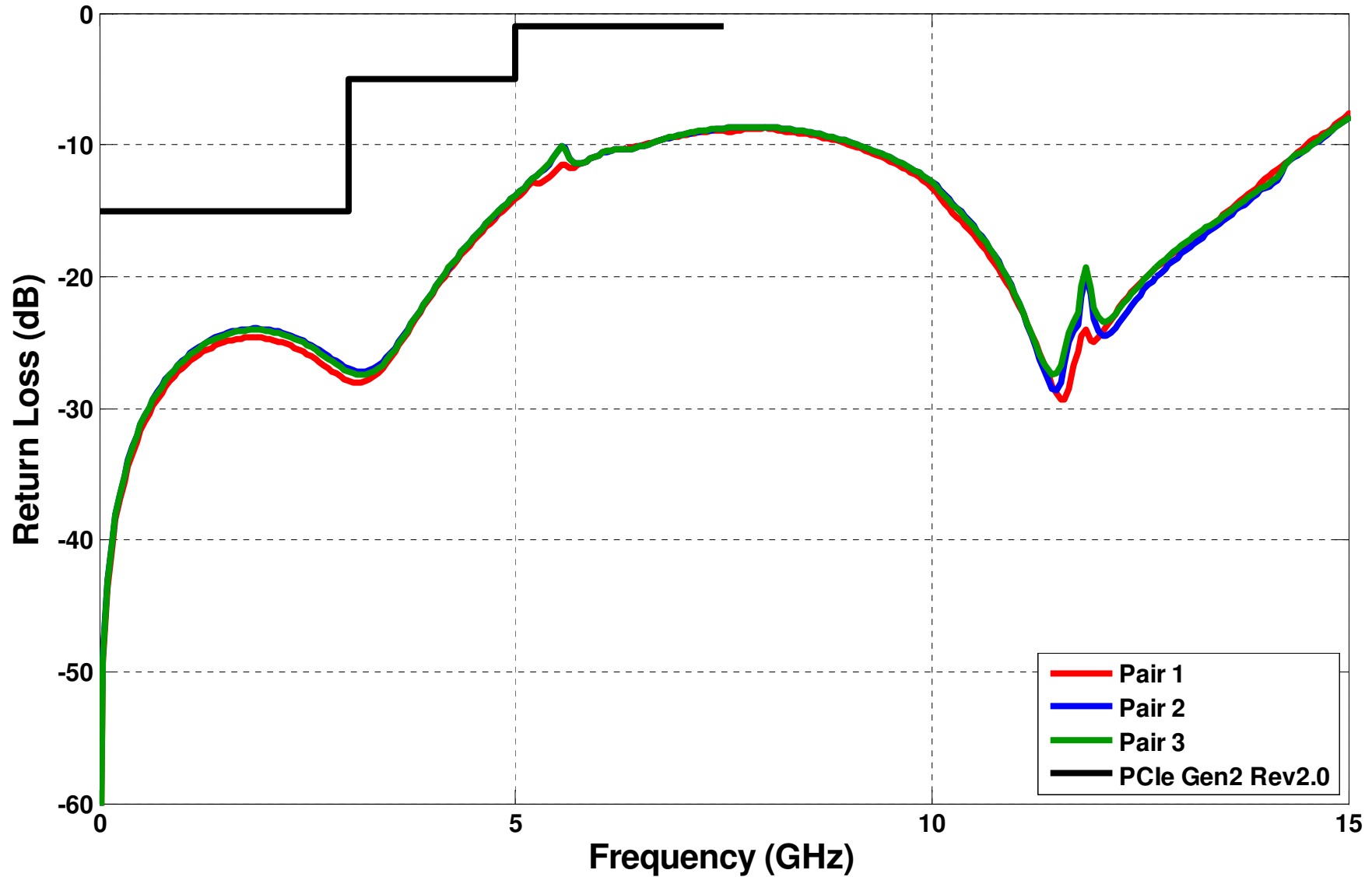
Bergstak 8mm - DIFFERENTIAL IMPEDANCE - Risetime = 50 ps (10-90%)



Differential Return Loss (GSSG)



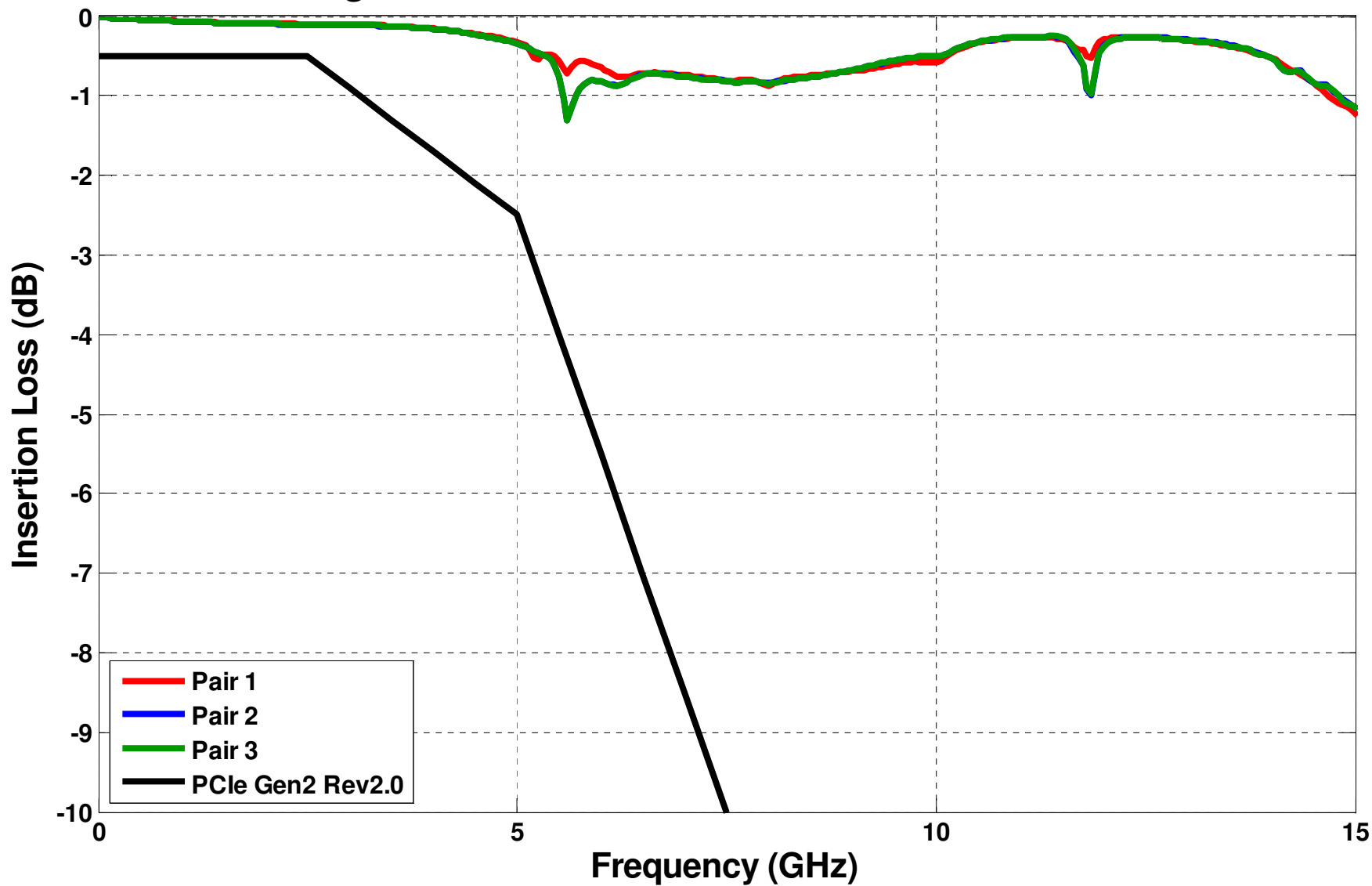
Bergstak 8mm - DIFFERENTIAL RETURN LOSS



Differential Insertion Loss (GSSG)



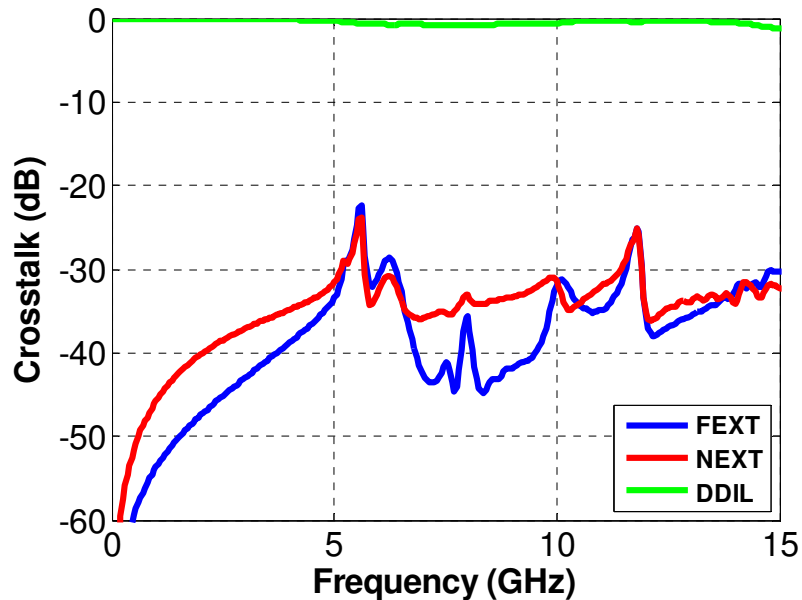
Bergstak 8mm - DIFFERENTIAL INSERTION LOSS



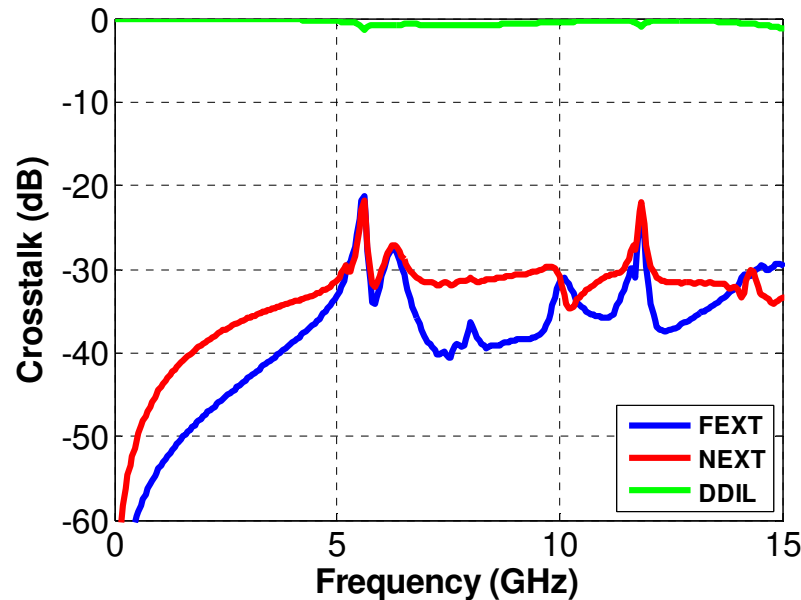
Power-Summed Crosstalk (GSSG)



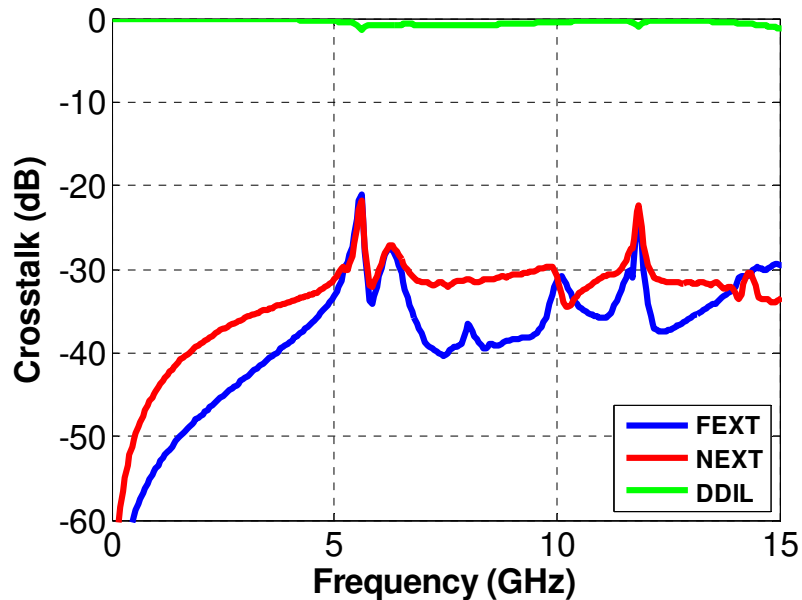
Pair 1 - POWER SUM X-TALK



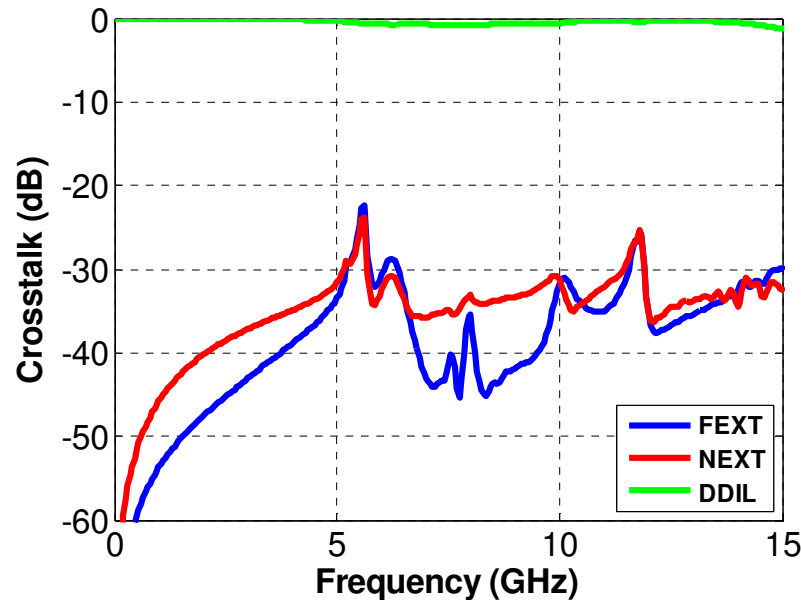
Pair 2 - POWER SUM X-TALK



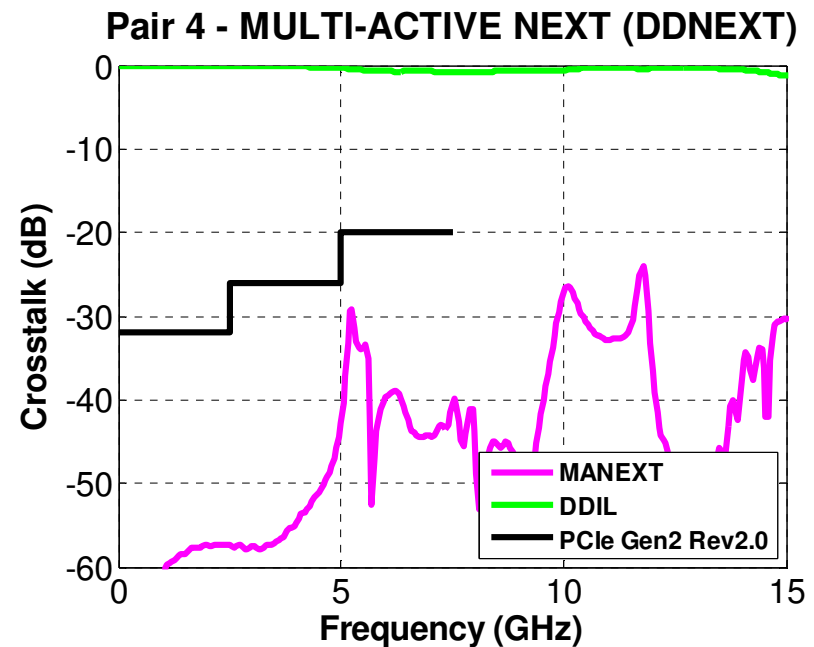
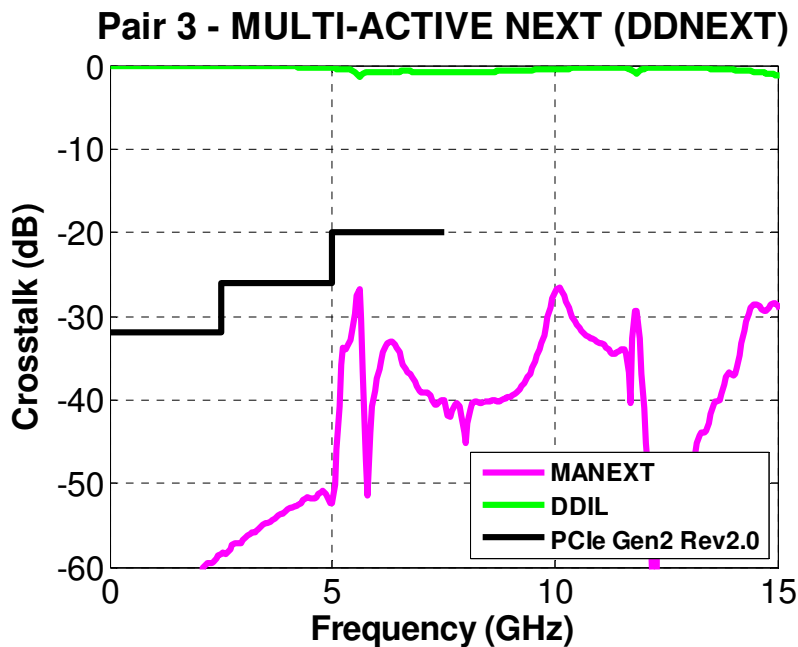
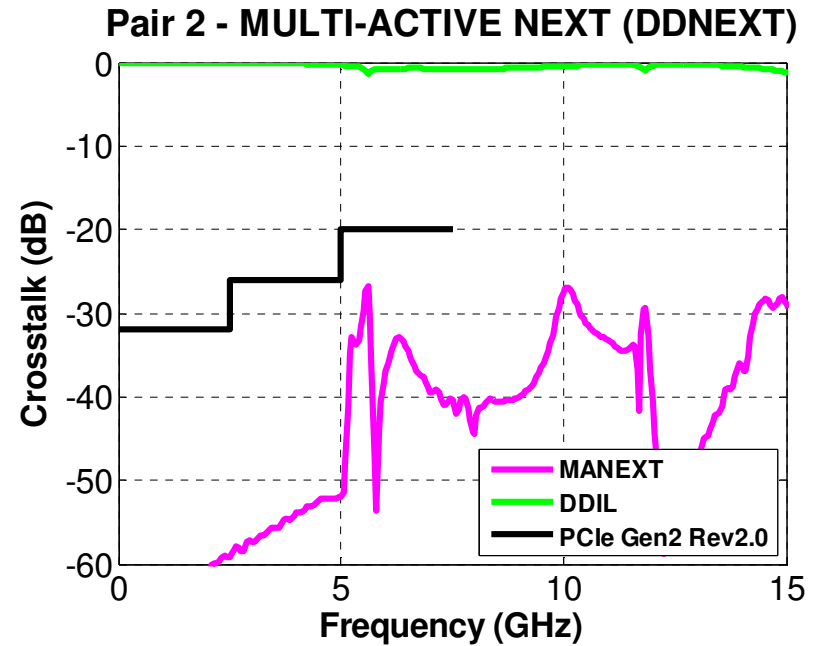
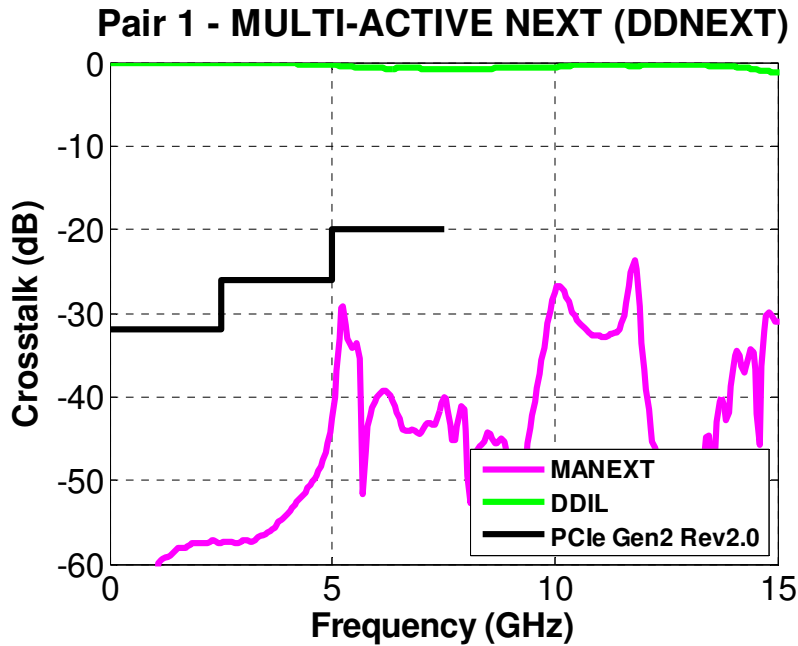
Pair 3 - POWER SUM X-TALK



Pair 4 - POWER SUM X-TALK



Multi-active Crosstalk (GSSG)



- BergStak[®] 0.8mm Mezzanine connectors , with a stack height of 8mm using this wiring pattern, meet the return loss, insertion loss and cross talk requirements of PCIe[®] Gen 2.

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The PCIe[®] mark is a registered trademark of the PCI-SIG Corp.