

## **Customer Simulation Report:**

# **MezzoStak™ 0.5 mm Mezzanine Connectors 7mm Stack Height vs. PCIe® Gen 2**

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## ***Purpose:***

- To compare the performance of MezzoStak™ Connector 7 mm stack height against the PCIe® Gen 2 specification
  - PCIe® Gen 2 Specification
    - 85 ohm reference impedance
    - Data rate: 5 GT/s
- Additional data such as impedance and power-summed crosstalk, which are not part of the PCIe® Gen 2 specifications, are also shown.

## ***Conclusions:***

- MezzoStak™ maximum stack height 7mm connector meets the PCIe® Gen 2 specifications
- Shorter stack heights will perform better, as the crosstalk resonance will move higher in frequency.

Table 5-3: Signal Integrity Requirements and Test Procedures for 5 GT/s Support

| Parameter                                | Procedure  | Requirements  |
|--|--|---|
| Differential Insertion Loss (DDIL)       | EIA 364-101<br>The EIA standard shall be used with the following considerations:<br>1. The measured differential S parameter shall be referenced to an 85 Ω differential impedance.<br>2. The test fixture shall meet the test fixture requirement defined in Section 5.4.2.<br>3. The test fixture effect shall be removed from the measured S parameters. Refer to Note 1.   | ≥-0.5 dB up to 2.5 GHz;<br>≥-[0.8*(f-2.5)+0.5] dB for 2.5 GHz < f ≤ 5 GHz (for example, ≥-2.5 dB at f = 5 GHz);<br>≥-[3.0*(f-5)+2.5] dB for 5 GHz < f ≤ 7.5 GHz (for example, ≥-10 dB at f = 7.5 GHz) |
| Differential Return Loss (DDRL)          | EIA 364-108<br>The EIA standard shall be used with the following considerations:<br>1. The measured differential S parameter shall be referenced to an 85 Ω differential impedance.<br>2. The test fixture shall meet the test fixture requirement in Section 5.4.2.<br>3. The test fixture effect shall be removed. Refer to Note 1.  | ≤ -15 dB up to 3.0 GHz;<br>≤ -5 dB for 3.0 GHz < f ≤ 5 GHz;<br>≤ -1 dB for 5.0 GHz < f ≤ 7.5 GHz  |
| Intra-pair Skew                          | Intra-pair skew must be achieved by design; measurement not required.  | 5 ps max  |
| Differential Near End Crosstalk (DDNEXT) | EIA 364-90<br>The EIA standard must be used with the following considerations:<br>1. The crosstalk requirement is with respect to all the adjacent differential pairs including the crosstalk from opposite sides of the connector, as illustrated in Figure 5-4.<br>2. This is a differential crosstalk requirement between a victim differential signal pair and all of its adjacent differential signal pairs. The measured differential S parameter shall be referenced to an 85 Ω differential impedance. | ≤ -32 dB up to 2.5 GHz;<br>≤ -26 dB for 2.5 GHz < f ≤ 5.0 GHz;<br>≤ -20 dB for 5.0 GHz < f ≤ 7.5 GHz  |

Notes:

1. The specified S parameters requirements are for connector only, not including the test fixture effect. While the TRL calibration method is recommended, other calibration methods are allowed.

PCIe<sup>®</sup> Gen 2 (5.0 GT/s) specifies the following electrical requirements

- Differential Insertion Loss
- Differential Return Loss
- Intra-pair Skew
- Differential multi-active NEXT

NOTE:

- Reference impedance for these requirements is **85 ohms**
- Specification applies only to the connector interface (which includes the **connector and the edge finger pads**). Other fixture effects must be removed.

- Historically, the power-sum method has been used to calculate the sum of crosstalks from multiple aggressors

$$\text{Power Sum } XT = 10 \log_{10} \left( \sum_n |XT_n|^2 \right)$$

- In PCIe specifications, an alternative method has been used to calculate the crosstalk sum (referred to as “DDNEXT” or “Multi-active Crosstalk” in this report)

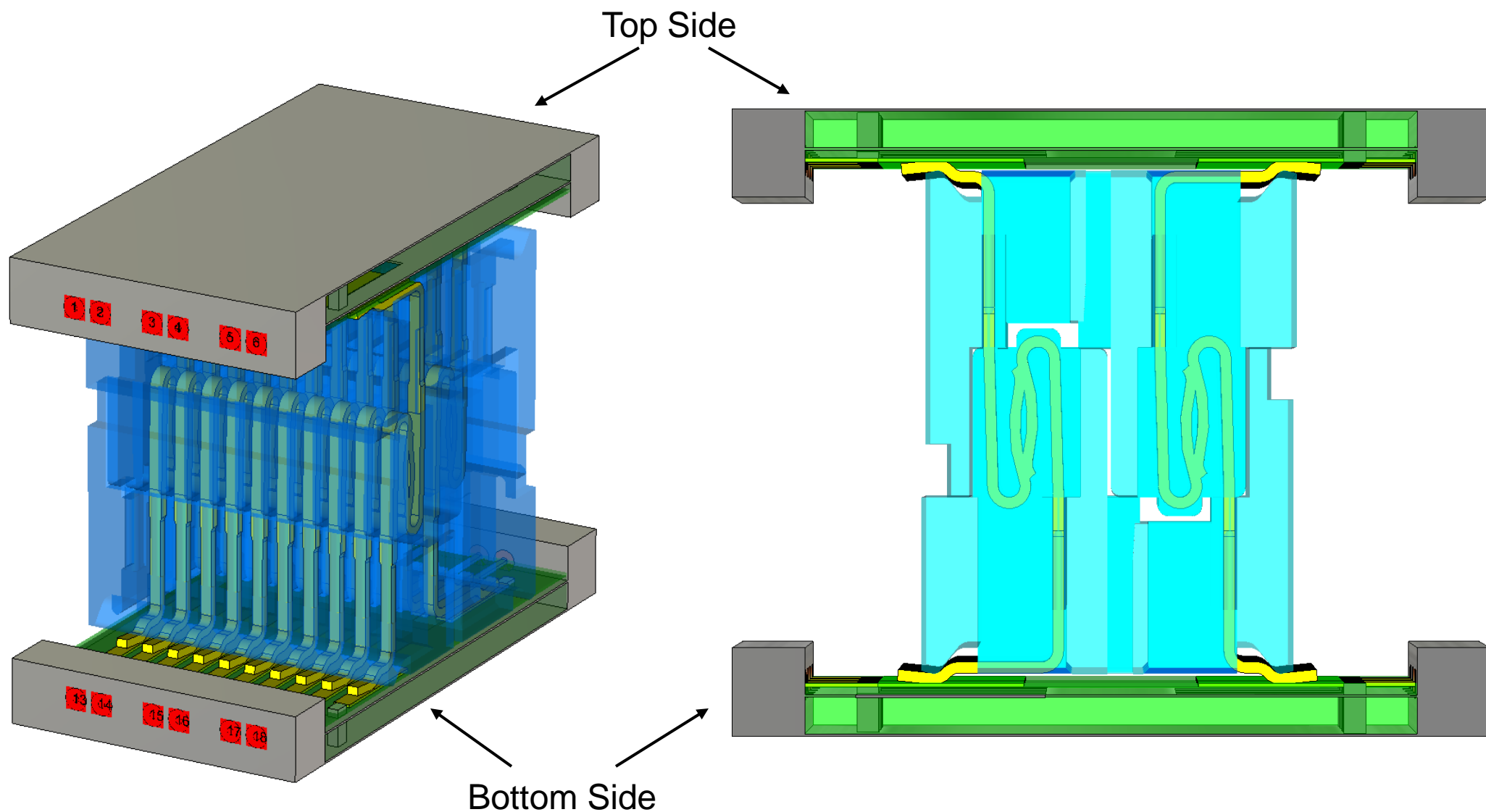
$$XT \text{ Sum } PCIe = 20 \log_{10} \left( \sum_n XT_n \right)$$

Where  $XT_n$  is the differential crosstalk S-parameter from aggressor #n

- Both power-summed and multi-active crosstalk plots are shown in this report

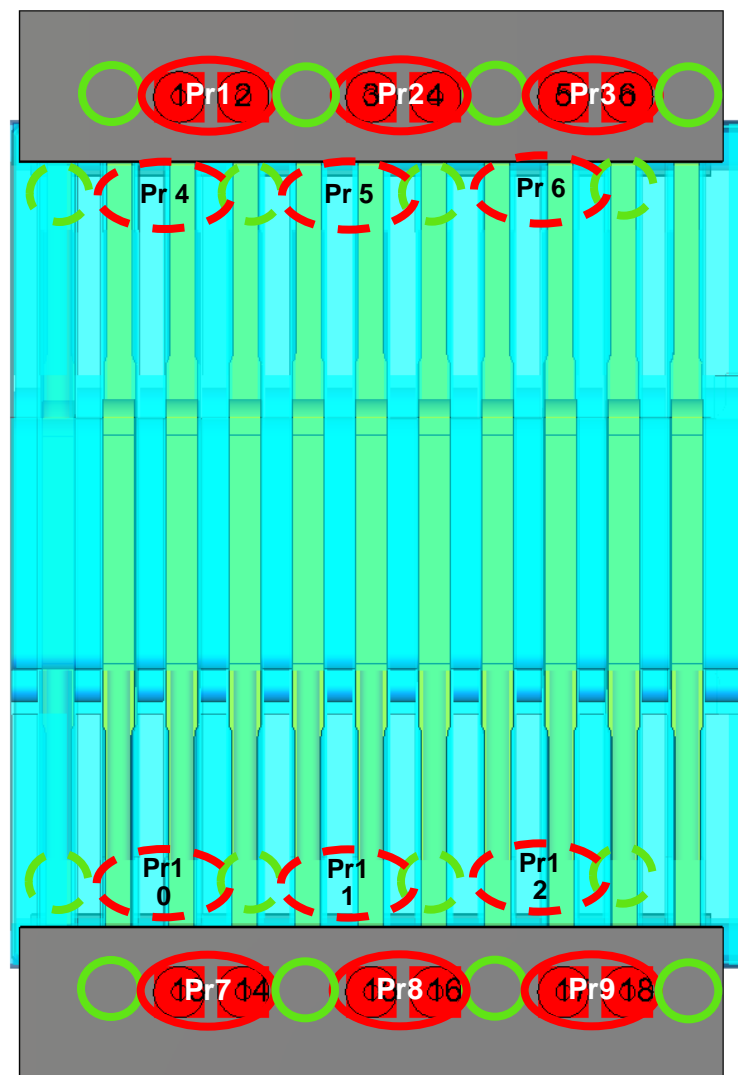
- The 3D geometries were solved using CST® MWS 2009.7
- Details of Touchstone file used in this report:
  - Filename:
    - GSSG: “mezzostak\_7mm\_20g\_gssg\_v1\_woren.s24p”
  - Frequency range: 0 to 20.05 GHz
  - Number of frequency points: 1001
  - Port reference impedance: 50 ohms
  - The Touchstone file was renormalized to a reference impedance of 42.5 ohms for the purposes of creating this report
    - A Touchstone file renormalized to 42.5 ohms is available upon request

# Geometry – 3D Views



50-ohm coaxial ports were used launch signals which created 100-ohms differential pairs  
GSSG geometry shown here as an example.

# Geometry – Port Definitions



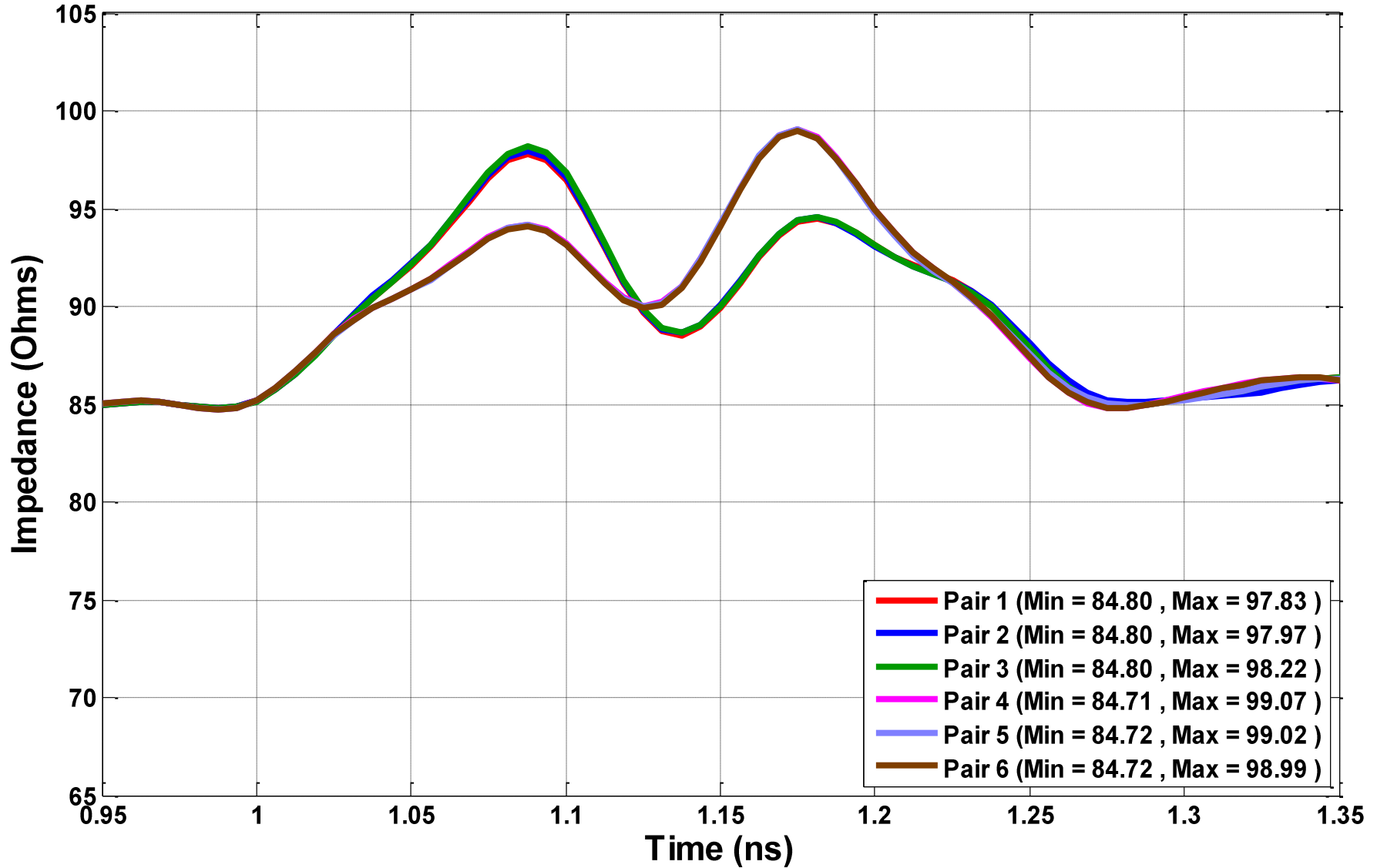
Dashed lines show pairs on opposite side.

**GSSG Pair Pattern  
(Opposite Side Offset by One Pin)  
Pair 1 connects to Pair 7 etc.,**

# Differential Impedance



MezzoStak 7mm GSSG - DIFFERENTIAL IMPEDANCE - Risetime = 50 ps (10-90%)

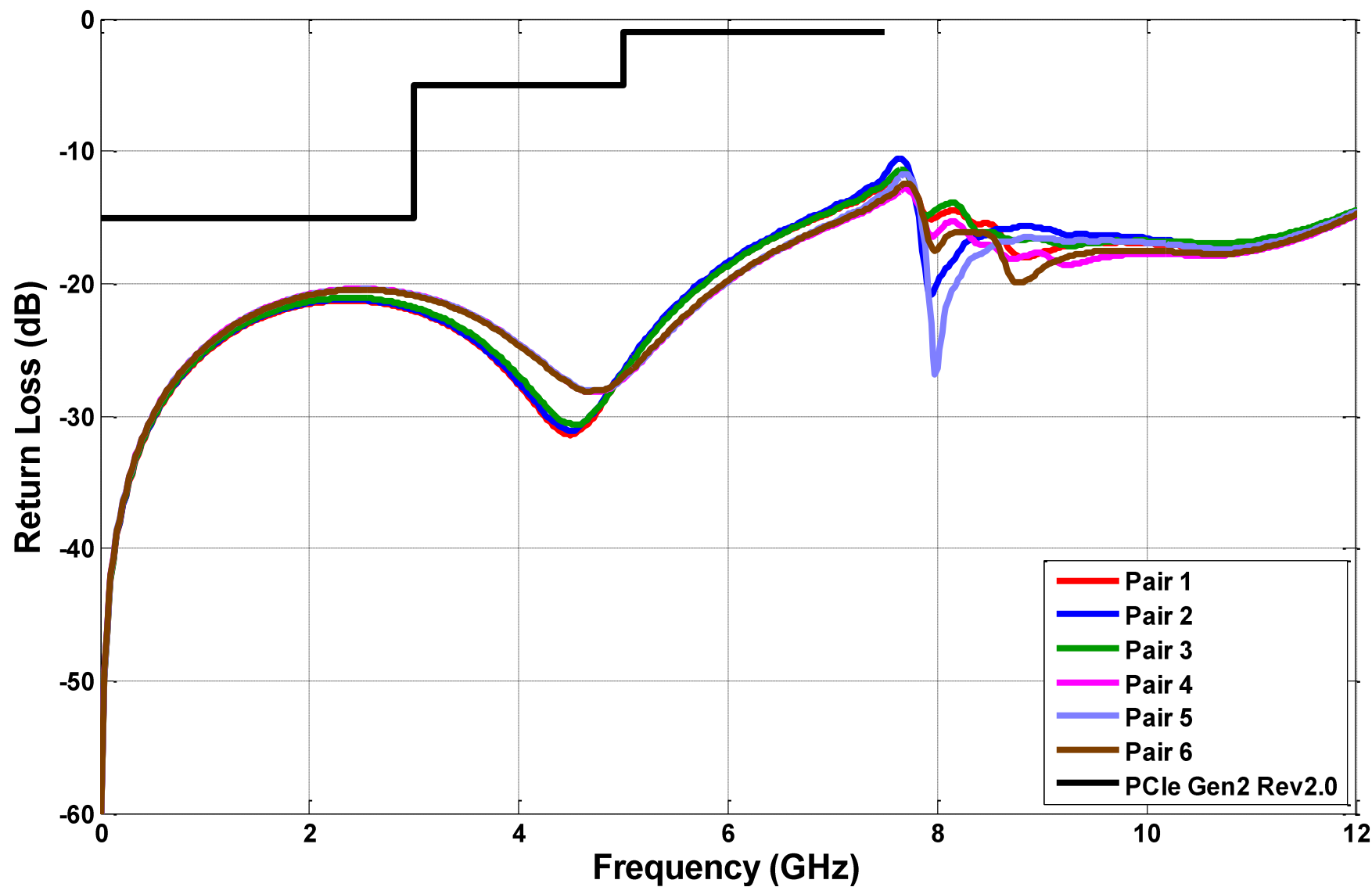


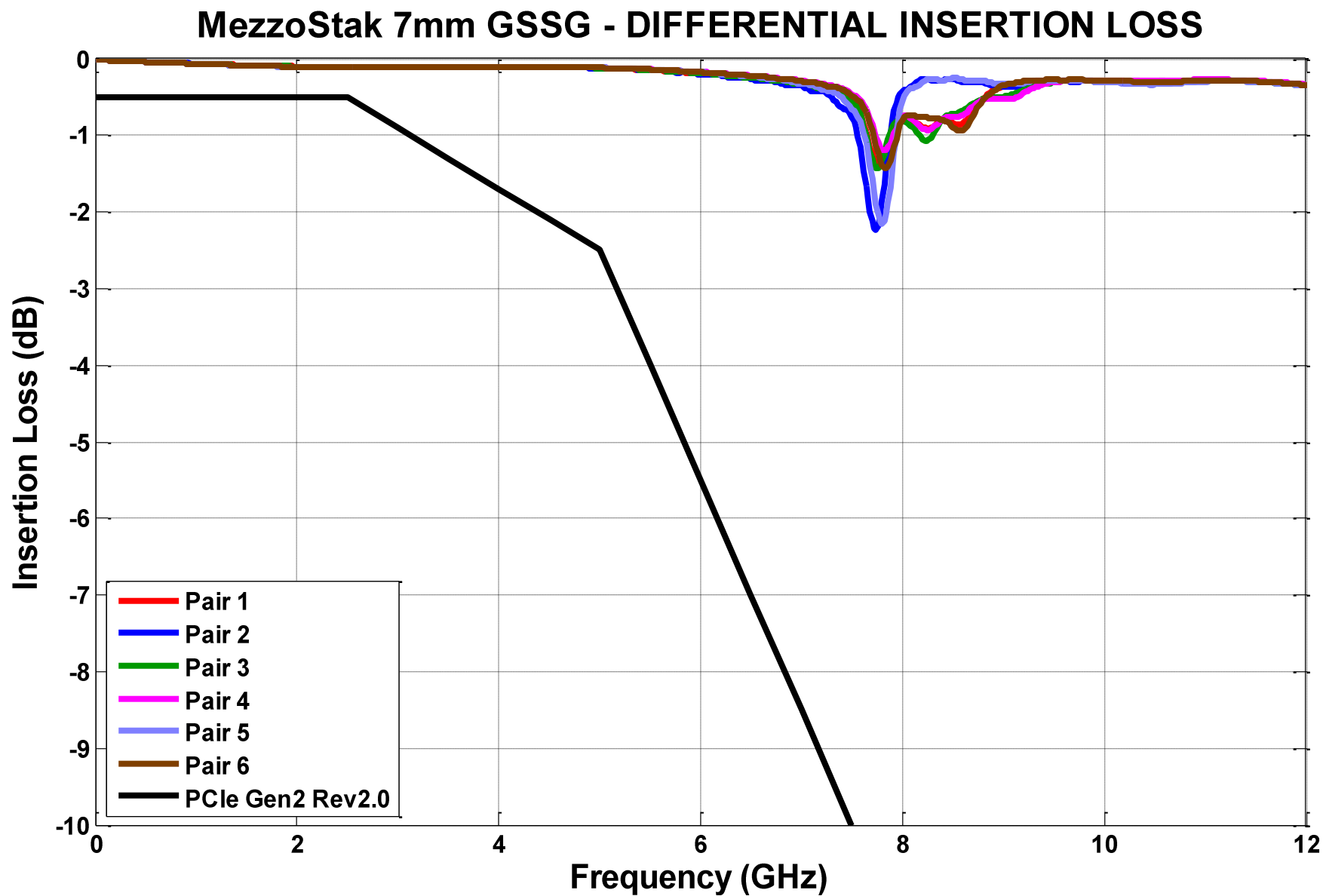
Impedance is not part of the requirement. It is given as additional information.

# Differential Return Loss



## MezzoStak 7mm GSSG - DIFFERENTIAL RETURN LOSS





# In-pair Skew (at 5% and 50% Levels)

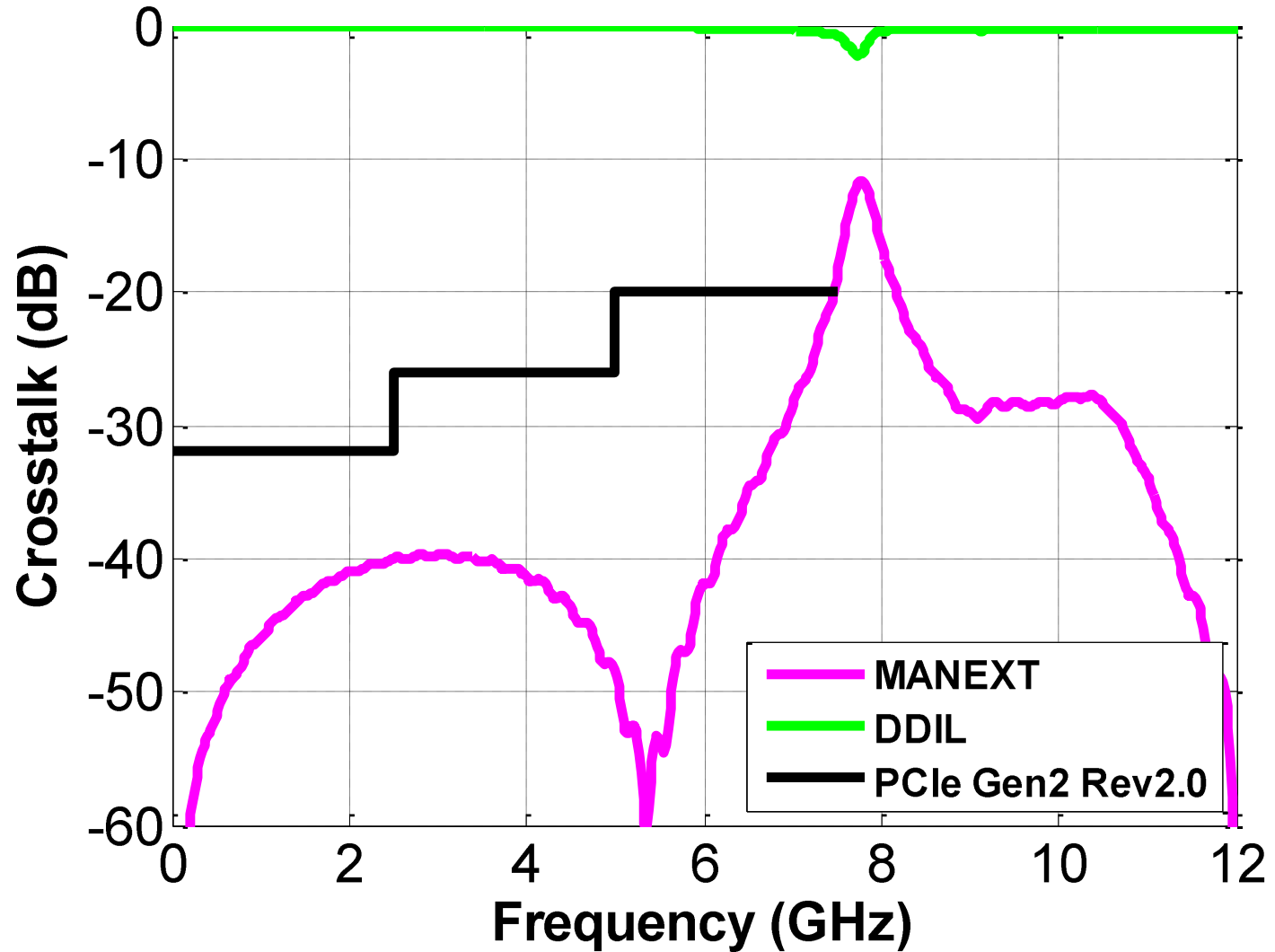


| MezzoStak 7mm GSSG - INTRA-PAIR SKEW [ps] |                           |
|---|---------------------------|
|   | Risetime = 50 ps (10-90%) |
|   | Level = 5 %               |
| Pin 1 / Pin 2                             | -0                        |
| Pin 3 / Pin 4                             | 0                         |
| Pin 5 / Pin 6                             | 0                         |
| Pin 7 / Pin 8                             | -0                        |
| Pin 9 / Pin 10                            | -0                        |
| Pin 11 / Pin 12                           | 0                         |

| MezzoStak 7mm GSSG - INTRA-PAIR SKEW [ps] |                           |
|---|---------------------------|
|   | Risetime = 50 ps (10-90%) |
|   | Level = 50 %              |
| Pin 1 / Pin 2                             | -0                        |
| Pin 3 / Pin 4                             | 0                         |
| Pin 5 / Pin 6                             | 0                         |
| Pin 7 / Pin 8                             | -0                        |
| Pin 9 / Pin 10                            | -0                        |
| Pin 11 / Pin 12                           | 0                         |

Connector has zero in-pair skew by design

## Pair 2 - MULTI-ACTIVE NEXT (DDNEXT)

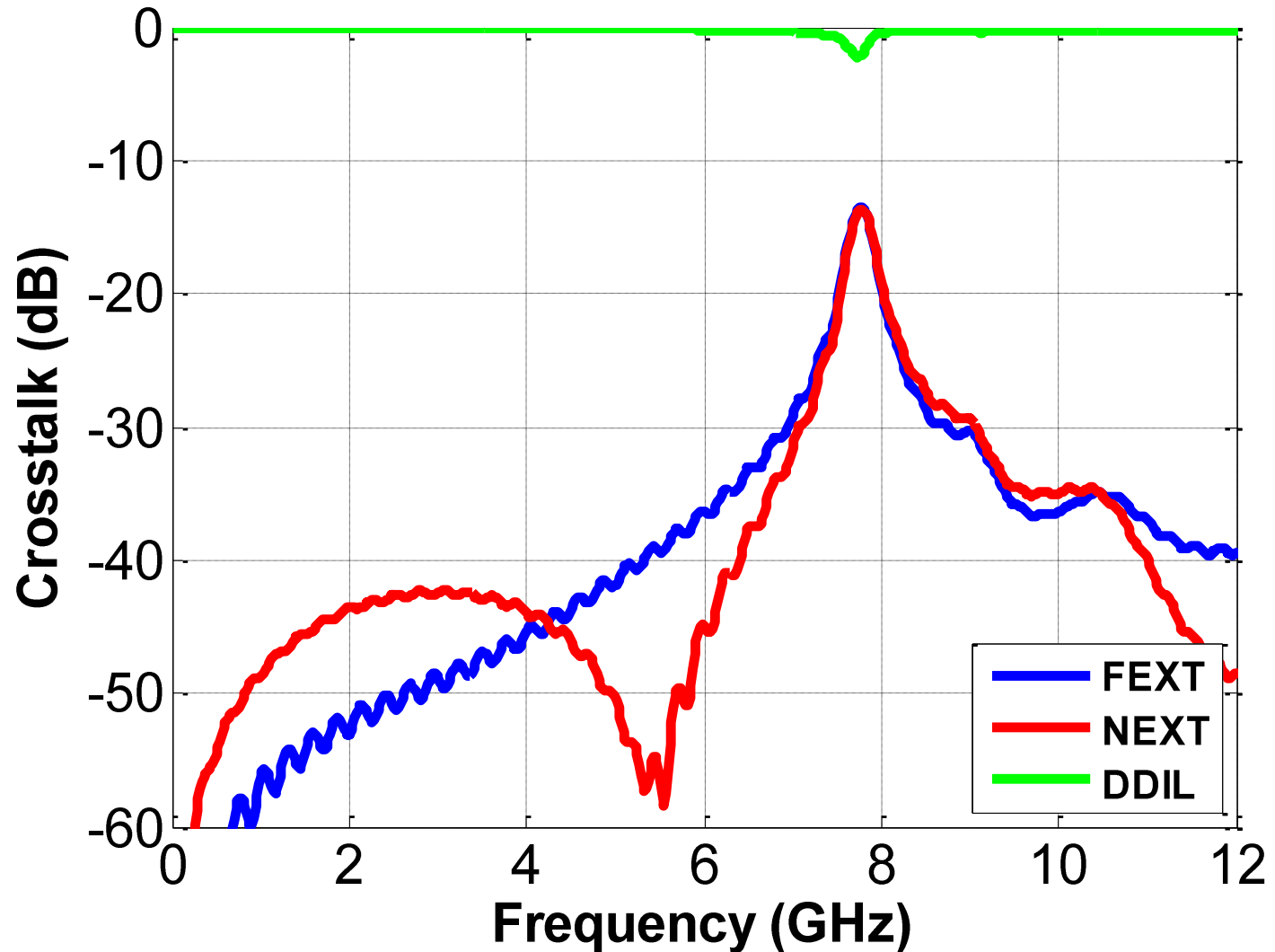
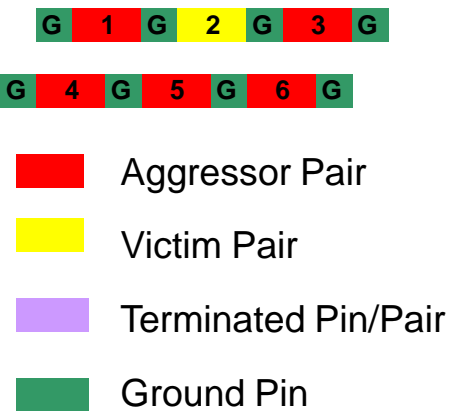


G 1 G 2 G 3 G

G 4 G 5 G 6 G

- Aggressor Pair
- Victim Pair
- Terminated Pin/Pair
- Ground Pin

## Pair 2 - POWER SUM X-TALK



Power-summed crosstalk is not part of the requirement. It is given as additional information.